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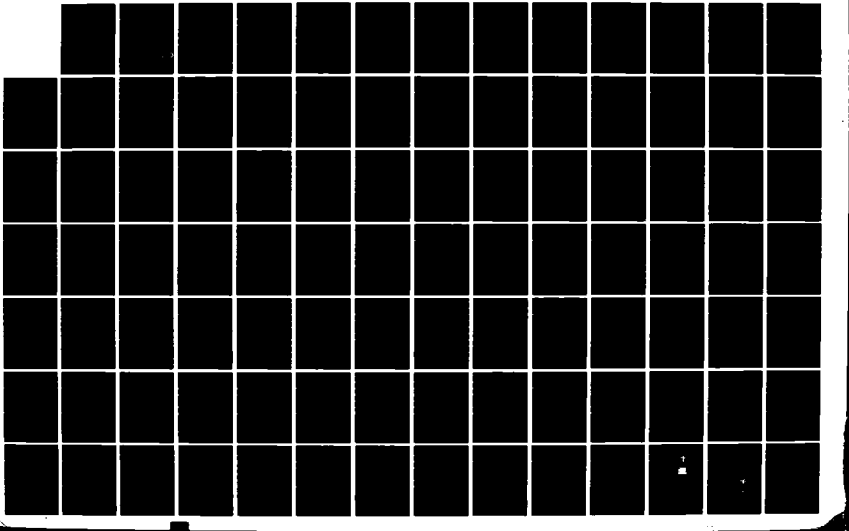

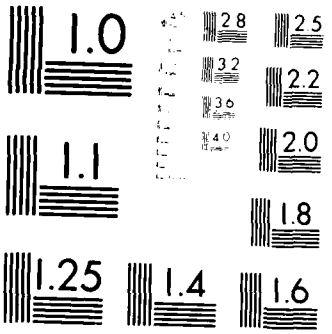

A COMMUNICATIONS LINK FOR AN IMPLANTABLE ELECTRODE ARRAY

THESIS

AFIT/GE/ENG/84D-70 Gregory S. Zeman
2Lt. USAF

DEPARTMENT OF THE AIR FORCE
AIR UNIVERSITY
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Wright-Patterson Air Force Base, Ohio

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Presented to the Faculty of the School of Engineering
of the Air Force Institute of Technology
Air University
In Partial Fulfillment of the
Requirements for the Degree of
Master of Science

by
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Second Lieutenant, USAF
December 1984

Preface

Man's ability to extract from a visual scene the simple essence which distinguishes an A from a B or a chair from a table is very much unknown. The ease at which the human visual system performs such pattern recognition has lead to the fundamental research in determining how man's brain performs such a task. Knowing some of the anatomy and the structure of the brain has not given a clear indication of the transforms and algorithms used. By providing a means to probe the visual pathway, where the measuring technique does not effect the natural response, the researcher might begin to understand the process which provides pattern recognition. Improving the techniques used might unlock more of the secrets hidden in the entire cerebral cortex.

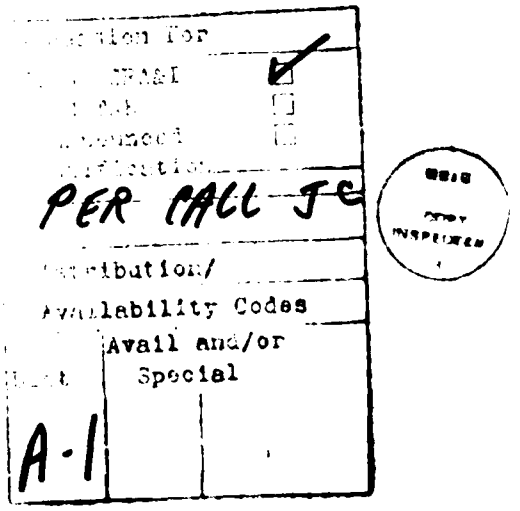
Each small advance in a field of so many unknowns generates so many more questions to be answered. The development of a small semiconductor electrode array as a tool for brain research gives rise to the question of how to make a system totally implantable for long term investigation. This research concerns itself with proving the feasibility of a completely implanted system for data collection using the AFIT 16 by 16 fully multiplexed electrode array. Once a system is implemented and cortical information readily available, others can unravel the transformations and algorithms which will model the visual system.

Special thanks are due to Dr. Dean C. Jeutter of Marquette University for his permission to use his transcutaneous radio frequency powering system and the help he gave in making a working breadboarded system. For Leroy Plynale and his colleagues of Hangar 4B, a note of gratitude for the help in working out the problems in the breadboarded RF powering system and for winding those ever elusive inductors.

My appreciation goes out to Dr. Matthew Kabrisky for his close support and guidance which gave direction and an element of learning to this thesis effort

Of special importance is the gratitude to my wife, Jane, who's endless hours of help in producing this manuscript made it all possible. And for understanding of the long hours of separation during study and research, I thank you.

Gregory S. Zeman



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Abstract

The research conducted in this study develops an implantable communications (biotelemetry) link for the Air Force Institute of Technology's implantable, multiplexed, multielectrode array used to record electric potentials on the visual cortex of a mammal. A prototype is developed to test the feasibility of transcutaneous data transfer and power transfer for a system relaying 100 KHz of data bandwidth. The working system uses a varactor FM modulator, phase locked loop demodulator, and op amp signal amplification. Power transfer is made by a single frequency RF inductive couple to an implanted rechargable Ni-Cd battery pack. The implanted system draws 18 milliwatts of power and the power supply is capable of supplying 30 milliamps of current at 5 volts for a 2 hour period before recharging is required. Details of the design procedures as well as recommendations for an implantable system realization are included.

[illegible] system. To do this the implant must provide support for the electrode array by supplying power and clocking to the array.

The system design must lead to a system which has biologically compatibility with the host. Size is a primary consideration in making a system conform to ultimate miniaturization and implantation which in turn dictates a small power supply. This forces low power designs, especially since substantial power drain occurs due to the NMOS electrode array, an unchangable part of the system. The power supply must also be able to supply voltages consistently over the entire time of operation. Operation in the body requires that the system does not damage the tissue or significantly alter natural functioning of the host . Therefore, techniques of encapsulation and trauma prevention must be addressed in the design.

A final part of the problem of an implantable communications link is reliability within the harsh environment of the body. Reliability requirements suggest simplicity in design, however trade-offs in performance must be made to accomplish it. Preventative measures in addition to circuit design are involved in solving the problem.

Scope

In order to achieve a working prototype of the initial biotelemetry link, existing designs will be used as much as possible. At radio frequencies, design is difficult to

power design which result in loss of programmable speeds.

Problem

The problem which is addressed in this thesis is the prototyping and evaluation of an outward communications link for the NMOS 16 x 16 AFIT electrode array. The communications link must supply the required power and clocking signals to the electrode array chip, provide amplification of the multiplexed brain signal, and modulate a radio frequency carrier suitable for detection and demultiplexing outside of the body. All processing must be done within low power constraints and be capable of reduction into an implantable system. The outputted signal must be decodable and the signals of each electrode reconstructed. The following paragraphs gives a more thorough description of the problem.

To provide a long term natural environment for the collection of electroencephalographic data from the visual cortex , an implantable biotelemetry link must be developed to interface with the AFIT 16 by 16 electrode array . This system must be able to take a pulse amplitude, time division multiplexed signal and process it so it can be transmitted through the skin and decoded outside. Information required for decoding must allow the determination of which electrode produced a particular voltage and when a change of electrode occurs. The unit has to supply electroencephalographic data for several hours at a time and be usable over a period of

Biological transmitters The use of biological transmitters is common for the study of electrical potentials in the body. As early as 1957 small FM and AM modulated signals were being produced by implantable transmitters for the recording of internal temperature. Small, battery powered units gradually emerged, which transmitted electrocardiogram and electroencephalogram data. The numbers of different transmitters produced in the 60's and 70's make it difficult to go into depth for each transmitter, but they can be generalized by the following characteristics; one to fifteen channels of low bandwidth signals, FM modulation using colpitts oscillators usually in the commercial FM band, and signal encoding of either pulse amplitude or pulse duration modulation. Other forms of tramsmission have been used, but the literature shows only a few of each. The circuitry over the years has changed from discrete components to integrated circuits (IC's), however the final output RF transmitter is still a single discrete transistor in most cases.

Evolution of the transmitter circuitry is dominated by the development of low power integrated amplifiers and CMOS digital control logic. This has allowed complex signal processing in the implant, making possible the monitoring of many signals (less than 15). Along with the development of high density IC's, the use of thick film substrate techniques have produced compact and highly reliable systems. The only limit on complexity of the system are power demand and low

materials using different application thickness and techniques, and found that phosphorsilicate glass (PSG) and polyimide produced the best resistance to ion penetration (14:38, 55, 59). In testing the array, he built drive circuitry which would eventually be used in an in vivo testing in a dog.

Armed with the devices produced by Fitzgerald and the passivation technique developed by German, the team of Russel Hensley and David C. Denton, GE-82D packaged a brain chip with interconnection to external support circuitry and amplification. Their thesis provides actual data on the fine grain electrode array used on the visual cortex of a mammalian dog. Although no detailed data reduction was performed, the thesis did provide the fundamental technique for surgical implantation of the brain chip electrodes, apparatus for data gathering of signals, and a method for the visual evoked response (VER) collection of data (15:10-11, 28-51, 64-66, 71-82, 86-89).

Successive theses in this area have tried to improve upon the inherent problems of JFET technologies by using NMOS arrays to produce both larger arrays and onboard multiplexing of the signals. These attempts have had some limited success towards producing a completely functional design. Once a larger array is fully operational, the problem of a fully implantable system arises where all necessary support and communication links can be contained in the host's body.

three theses at the Air Force Institute of Technology which developed an implantable semiconductor electrode array and successfully used the device in a dog. The work in the progression is summarized in the following paragraphs.

The initial proposal for a AFIT multielectrode array come from Joseph Tatman, GE-79D. His proposal was the development of an electrode array using JFET technology to be used in conjunction with a multiplexing scheme, voltage amplification, and pulse duration modulation using a tunnel diode oscillator. Although Tatman's array did not work, he laid out the fundamental requirements for a large scale multielectrode array using biotelemetry and transcutaneous power coupling to the implanted device (5:22-44, 80-86).

Gary Fitzgerald, GE-80D, continued the work started by Tatman in developing an electrode array. Fitzgerald's work incorporated a new fabrication process to remove problems found in Tatman's array. Also included in his thesis effort was a change of electrode metal from gold to silver-silverchloride to produce better electrode response. The electrode array did work on air but failed in the sodium ion rich environment used to simulate the brain (13:108-109).

George German, GE-81D, took Fitzgerald's arrays and sought a passivation method for the array which would solve the problem of ion contamination of JFET switching transitors while having suitable dielectric and water absorption characteristics necessary for semiconductor design. After evaluating the source of contamination, German tested 5

multiplexing of electrode arrays is the substantial reduction in the number of output leads and the reproducibility of each electrode within an array.

The electrode array produced at The University of Southampton, England in 1980, shows great foresight into solving some of the problems associated with recording of biological signals. Their array is a 9 electrode (3 x 3) array built around MOS technology where the electrode itself is the metal gate for a transistor which provides initial amplification before noise effects can materialize and an impedance match for the high source impedance found when reading electric potentials off the brain. The output of each electrode drives a source follower configuration which is directly coupled into a voltage amplifier. The problem of insulation of active devices and leads from water, salt, and other ionic damage is provided by silicon dioxide, positive photoresist and varnish depending on the exact area of the chip (11:553-556). To limit the number of output leads multiplexing circuits produced a single pulse amplitude modulated, time division multiplexed signal which was passed out of the brain using wires. The quality of the signals achieved was above what was gathered using glass pipette methods. This work proved to be very much similar to the work being done at the Air Force Institute of Technology.

AFIT Electrode Array Research. Parallel to the Jobling experiments in England were the sequence of Masters

with various stimuli. The technique proved successful, but the large bundles of wire made the devices very sensitive to breakage, very hard to reproduce identical characteristics for each probe and producing 400 amplifiers to read the data is impractical. Other problems included crosstalk between adjacent electrodes and the shear physical bulk of the apparatus, especially in the brain cavity. The results of this study showed evidence that the activity from a evoked response is very localized, at least as small as .5mm (the resolution of the system) and not distributed as some earlier EEG techniques had seem to shown (9:23-24, 26-29). This reduced grain size analysis is now the basis for the AFIT and University of Southampton semiconductor electrode arrays.

Electrode Arrays. The present state of the art for electroencephalographic recording of the cortex is the semiconductor electrode array. Separate but concurrent work in this area by bioengineering students at the Air Force Institute of Technology and researchers at The University of Southampton, England, proved the use of semiconductor technologies in the manufacture of fine grain electro-encephalographic electrodes. The designs of each array, although quite different, demonstrated the principles introduced by Wise in his multielectrode array using photo-lithographic methods to define electrode and active devices (10:238-239). The significant achievement of each of the

Part 1: Introduction to Electroencephalographic Studies.

fully interpret the BCE interconnections by measuring evoked electric potentials, a small reliable electrode capable of measuring small potentials in a localized area was needed. This section will describe the evolution of the research from single probes to large semiconductor electrode arrays.

Brain activity in early research was measured by cumulative responses of many neurons measured by large electrodes on the scalp. This provided very basic information but lacks the detail needed to generate models of the brain. The next level of research was done using single cell microprobes made of relatively inert metal wires or glass micropipettes. These probes were inserted directly into the brain tissue so the tip of the electrode penetrates neural cells. The electrodes produced excellent responses but physical damage to the cell creates unwanted responses not associated with the normal pathway. A typical example of this is the work done by Hubel and Weisel in the cortex of a cat and monkey (8:106-110; 6:153-159). Measurements of this type were very useful in determining a size associated with a BCE.

Research then moved towards an electrode array to measure evoked potentials over a large area of the visual cortex but in sufficiently fine detail. Fine wire electrodes were bundled into an array to produce a uniform pattern in which potential gradients across the surface could be measured. The work done by DeMott used a 400 probe array to

cortex produce fixed point sources, not complex shaped visual patterns (7:106-108). Further, these experiments imply the perception processing of the brain is not done within the primary visual area, but rather a process of the pathways after this point. Secondary visual cortex simulation by electrodes has caused complex shapes and patterns to be observed. This transition from point sources to complex line and shape patterns means that some level of perception occurs within that mapping.

The next level of research is the recording evoked potentials of individual BCE's which might give an averaged level of activity of the neurons composing a single BCE. BCE activity corresponds to direct neural stimulation of the BCE and gives a general way to monitor stimulation within the pathway. Electroencephalographic monitoring with electrodes provides a means of simultaneously recording electrical signals at sites in both primary and secondary areas, giving some information about the interconnections, but lacks in resolution. Alternative methods of determining mapping would be to do a Golgi-stain method and trace individual neural fibers. However, the time required to trace the millions of interconnections would seem to rule out this type of detailed anatomical study. This forces the more general study technique of electrode recording of BCE activity to produce some reasonable model of the mapping.

in visual areas. Through these observations it was possible to infer a direct mapping of the eye to the primary visual cortex and that the ultimate pattern recognition occurs, in part, in the secondary or association visual cortex. Concurrent work by anatomists found that the visual cortex areas perform processing on a very localized basis due to the lack of large scale spreading of nerves connected to an input nerve. These inferences were made from elaborate Golgi-Method staining methods used to determine localized neural networks (6:152). The localized processing units referred to by Kabrisky as the Basic Computational Elements (BCE) is the unit of interest in determining the exact processing nature of the cortex. It is believed that at this level the inputs and memory form a functional transformation of the information. However, the ability to trace signals by looking at single neurons is not easily accomplished, and research efforts have preceded to look at the interrelation between arrays of BCE's and the resulting transformation which contains fundamentals of perception (5:39-54).

The interconnection of the many BCE's of the primary visual cortex area to a single BCE of the secondary visual cortex implies a formal mapping transformation similar to those of a two dimensional Fourier transformation or similar transformations. Experiments performed by Brindley and Donaldson using electrical stimulation directly to the primary cortex produced spots of light known as phosphenes and shows that stimulation of BCE's of the primary visual

however, stimulation of the secondary visual cortex or a combination of the primary and secondary cortical areas could significantly reduce the number of stimulation points needed to produce a recognizable patterns. Because of the one to one mapping from the retina to the primary visual cortex, the amount of information which the optic nerve provides is prohibitively large to seek to simulate with electrode stimulation. If the transformation process which takes places at the secondary visual cortex could be tapped into producing a decoded pattern with only a few stimulation points, a reasonable facsimile of sight might be produced by external stimulation. A thorough analysis of the visual cortex may provide the means by which a practical visual prosthesis can produce quality limited visual sensation for many blind persons.

Background

The Visual Perception System. Neurological research directed towards understanding the function of perception, although extensive, shows little success into learning the methods used by the brain to extract perceptual information. Man's ability to recognize objects in a complex field, read handwriting from many different sources or perceive familiar shapes is relatively unknown. Many experimental methods have been pursued to fulfill a gradual understanding of the perception process. Early research into visual mapping came from observations of visual effects when brain damage occurs

the brain can be drawn.

As the mapping of the stimulus through the eye to the primary visual cortex is accomplished, experimental demonstration of a 1 to 1 mapping function of the eye to the primary visual cortex can be explored further. By placing two electrode arrays on the brain, one on the primary visual cortex and another on the secondary visual cortex it is possible to begin the task of mapping the neural response of the secondary visual cortex to that of primary visual cortex. This information is necessary to develop a model for the human visual system, much like the one proposed by Kabrisky, a two dimensional cross correlation (5:47-53, 58-59, 82). As suggested in Kabrisky's concluding remarks, "Finer details of the cortical connections are required to decide the case for either the proposed model or one computing with transforms (5:82)." This thesis will aid in achieving that finer detail needed to determine an appropriate model. Through direct application of such a model, a scheme for pattern recognition with a machine can produce results that rivals man's. As the model is refined and better understood, the model could be generalized to other sensory and thought processing done by the human brain.

As information on the visual pathway's interconnections and information processing techniques are unraveled, the reality of a limited visual prosthesis for the blind becomes a reality. Present work in the visual prosthesis area explores the primary visual cortical area for stimulation.

mapping relationship between the primary and secondary visual cortex, and ultimately find an effective way for external stimulation to provide limited sight in many blind persons (1:281-282; 2:14; 3:479; 4:44).

An extended implantation life for the implanted electrode array will allow a long term test period in which evoked responses can be measured from visual stimulation through the eye. This will prove especially important in determining the effects of enviromental changes on electroencephalographic data for similar stimuli. But more significantly, the use of a biotelemetry system will reduce the effects of localized trauma due to incisions needed to allow communications and support wires to pass out of the brain cavity. A completely implanted transmitter would allow the skull and skin to be completely closed after implantation. This allows the body to form an intact seal preventing bacterial infections which could prove dangerous to the subject. Not only is the chance of infection reduced but the localized area will gradually adjust to the presence of the implant, reducing the effects induced by the implant being within the brain cavity. By allowing the most natural response over a long period of time the experimental data will produce a consistent representation of the electrical physiological events in that localized area of the brain. Data free from perturbations due to the presence of measurement equipment should provide a sound and very realistic picture of the brain. With this type of data reasonable inferences concerning functioning of

A COMMUNICATIONS LINK FOR AN

IMPLANTABLE ELECTRODE ARRAY

I. INTRODUCTION

Significance

Neurological research over the past century has made major advances into understanding the functioning of mammalian brain. However significant the scientific research has been, only inferences can be drawn on exactly how sensory information is processed in the cerebral cortex and used to make decisions. The visual pathway is of particular interest because of the scientific community's limited understanding on how the brain is able to recognize particular shapes; either scaled to various sizes, rotated over a range of angles, located in a cluttered visual field, or just plain distorted. Understanding this process of information extraction from sensory information provided by the eye, could allow us to mimic the process on machines, to provide pattern recognition, or to intervene in the brain's natural process in order to help those whose vision has been impaired due to damage somewhere along the visual pathway. This effort is significant in that it will prove a design of a communication link which will allow extended implantation life for the Air Force Institute of Technology's brain electrode array, providing a simple means for establishing a

produce stable designs. Furthermore, designs will be sound but may not extend beyond the very simplest capabilities of the devices. Large bandwidth requirements of the PAM modulating signal will be reduced as much as possible to produce a working amplifier and waveshaping circuits which can be designed for a thick film realization for implantation. This thesis will make no attempt to produce an implantable system but rather show the feasibility of such a system and provide the guidelines for a system using what was learned in this prototype.

The design presented in this thesis makes several assumptions as a starting point of the design. First it is assumed that the system is to be used with a fully multiplexed 16 by 16 electrode array implemented in NMOS. The only required inputs to the array are power in the form of a ground and a positive supply between 3 and 6 volts, a clocking signal to sequence the array between electrodes, and the ability to use a power supply line to hold count-select and sync-in pins at proper values. Also assumed is that ample room exists in the receiving host to implant a small power supply and transmitter in the chest cavity and the electrode array assembly in the brain cavity. Finally, it is assumed that this thesis will not produce the circuitry necessary to reconstruct the signal at each electrode but rather it will supply the PAM signal and synchronization to decode the signal.

Testing of the system will be done on a breadboard where

array characteristics will be simulated with a waveform generator and with electric models for the electrodes. Power unit testing will demonstrate the ability to supply sufficient power to an internal battery pack.

Approach

The approach to solving the problem presented here is comprised of six major steps. Step one is an exhaustive literature search, where systems for biotelemetry and inductive power transfer will be explored and examined for suitable adaptation to the design problem. Step two will produce a design of a frequency modulated (FM) transmitter capable of transmitting the broadband pulse amplitude modulated (PAM) wave. This FM signal will be inductively coupled to a demodulator outside the brain cavity. The transmitter must also be breadboarded and tested to show ability to produce exceptable modulation even when inductive coupling coil is submerged in the lossy body fluid. Step three involves designing an amplifier for the EEG signals, and then adding sufficient synchronization information to provide suitable reconstruction of the signals. Once again this will be breadboarded and tested for stability and compatibility with the electrode array and the transmitter.

Step four is the development of an external power supply source and a means of generating a clock to sequence the array through each electrode position. System design will be adaptations of existing systems and will be breadboarded to

prove workability. Step five is the design of a simple FM receiver to reproduce the array's PAM waveform and the superimposed sync waveforms. The final step will integrate the entire system and test for ability to reproduce accurately the PAM waveform generated by the electrode array. At the time of this writing, a working fully multiplexed array does not exist so biological signals must be simulated to evaluate system performance so that recommendations can be made to improve the system design and provide system miniaturization for implant use. Once the system is evaluated, extensions of the system will be recommended.

Order of Presentation

Chapter two will present a detailed analysis of the problem, describing requirements and system trade-offs. Chapters three and four will discuss the actual design of the system, including the basic theory, the design procedure and the steps necessary to produce a working system. Chapter five will present the results of the system's testing and discuss attributes as well as problems. Chapter six will draw conclusions about the system and make recommendations for further research.

II. Detailed System Analysis

Theoretical Basis

As stated in the background section of this thesis, the manner by which the brain processes visual information to formulate pattern recognition within the brain is very much unknown. Previous work has shown a fundamental one-to-one mapping from the retina to the primary visual cortex and a more complex mapping from the primary visual cortex to the secondary or association areas. The work of DeMott and several AFIT theses has shown that processing of input stimulations occurs locally within the cortical layer and is then passed on by interconnections for further processing in subsequent areas. Because of this very localized computation being performed in the brain, individual areas of the brain (BCE's) can be monitored to reflect activity of computations being performed at small points in the map. This allows the mapping to be determined using a two dimensional array where the propagation of signals within the array reflects the computation performed and the interconnection of these BCE's. This is much easier to monitor than if the computation were done as a continuous propagation of a signal as it diffuses over an entire sheet of the cortex. The localized nature of the BCE's allows the use of electrode arrays to record activity of each BCE after a visual stimulus. As noted first by DeMott, and later by Hensley and Denton, large cortical

voltages (100 -200 μV) are observed between electrodes spaced as closely as 100 - 200 microns and can be easily multiplexed by the AFIT hardware.

Activity in a single BCE is composed of the firings of many neurons over a relatively short period of time. If these signals could be monitored in close proximity o individual cells , the frequency bandwidth would be several kilohertz. However, since monitoring is done a distance from the actual nerve endings and capacitively coupled to them, the net effect is to average the high frequency pulses into a slowly changing potential which indicates some measure of activity in each of the BCE's. The relatively low signal bandwidth of the electroencephalographic signal makes it possible for a time division multiplexed signal to be generated from the 256 electrodes in a 16 x 16 array which is narrow enough in bandwidth to be transmitted over a FM radio frequency carrier.

The purpose of this thesis is to test the feasibility of designing an implantable system which can take the time division multiplexed signal from the 16 x 16 electrode array and process it so it can be reconstructed outside the body while supplying necessary support (power and clocking) to run the array chip.

Problem Analysis

To test the cortex for patterned responses from predetermined stimuli, and ultimately use the data to track

preparation pulls, the cortical surface must be monitored over a large area of the visual cortex. The monitoring is accomplished by a large electrode array which must be able to simultaneously record signals generated at each location in the array. The system should be chronically implantable so that the recording can be done over significantly long periods of time and without the effect of anesthetic and antibiotic agents on the response of the visual pathway. Repetitive evoked responses can reduce random effects of noise and variance within experimental procedure to produce consistent and repeatable responses allowing well founded inferences to be drawn. When implanted, the unit should in no way interfere with the normal functioning of the biological host to insure results are not induced by the physical presence of the monitoring unit. Finally, the unit must be capable of monitoring a large area of the visual cortex, both primary and secondary areas. Monitoring of the total area would require hundreds of thousands of electrodes to monitor all the BCE's associated in the first two levels of signal processing within the visual pathway. At this level the design of a telemetry system reaches a limit to transmit all the information of each and every BCE. Because of the finite bandwidth of any communications channel built with currently available low power chips, only a small number of BCE's can be looked at one particular instant. The array cannot be physically moved further limiting the scope of what can be monitored.

Within the constraints of semiconductor technology and the ability to process only a finite number of electrode data sources, a 256 electrode array is a reasonable choice for implantation with a telemetry link. Other thesis efforts have produced electrode arrays capable of producing a multiplexed signal of electrode responses and tests have shown that devices are implantable and capable of sustained use in the hostile cerebral environment (see background in Chapter 1). At present, a 256 electrode array which is fully multiplexed has not been totally proven, however the design of the telemetry and powering links assumes a totally operational 256 electrode array. The detailed design presented in this thesis will show the feasibility of producing a low power large bandwidth telemetry link using commonly available IC chip sets. This thesis will not explore the possibilities of custom integrated circuits to produce necessary telemetry links as has been done by Stanford University's Kit Chip Project (16:91-98).

Presently, large scale integrated circuits have opened many possibilities of producing low power circuits to perform waveshaping, amplification, and control functions required for an implanted system. Complementary metal oxide semiconductor (CMOS) devices produce low power control logic and waveform generation, while low power optimized op amps produce reliable amplification. High frequency design of modulators still requires discrete transistor design, however, possibilities of large scale integrated circuit

phase locked loops offer an alternative to discrete component design. Ultimate design of the modulator depends on the power consumption of the modulator design. Once an exceptable outward transmitter is achieved, a receiver capable of demodulating the FM signal into its PAM representation will be designed. This design must extract the information needed to reconstruct the signal at each electrode. Devices used for the receiver are external to the host allowing for a relaxed power constraint and a wider choice of commercially available IC's to perform the demodulation. Simplicity in both internal and external parts of the communication link facilitates ease of construction, reduction of size, and most importantly, increased reliability of the entire system. It's within these constraints that a more detailed analysis of the problem is undertaken.

System Requirements

Objectives.

1. Provide impedance match of brain electrodes to the PAM amplifier.

2. Provide amplification of time division multiplexed signals provided by the electrode array so both voltage and impedance are acceptable for the modulator.

3. Provide synchronization marks within the PAM signal to indicate electrode position with respect to actual voltage output.

4. Provide necessary clocking for electrode multiplex sequencing.

5. Provide the required low voltage and low current supply.

6. Provide transcutaneous power transfer to rechargable battery source.

7. Provide a design scalable to thick film circuitry for chest cavity implantation.

8. Provide long life time and reliability.

9. Provide a reasonably accurate reproduction of PAM signal (minimum noise) before demultiplexing into individual electrode signals.

These objectives provide the basic requirements needed to achieve a long term implantable telemetry link. Conflicts between objectives lead to compromise of these objectives. Trade-off areas are power consumption, noise, simplicity, and signal bandwidth. Within the detailed design these facets of the system are traded off until a nearly optimum system is produced.

System Overview. The system design from a block diagram point of view can be readily seen from the block diagram in figure 2.1. The system is divided into three functional blocks: (1.) Signal Processing and FM Modulation, (2.) FM Demodulation, and (3.) Power supply and Support Circuitry. Composing the signal processing and modulator segments is an amplifier capable of bringing the low level brain signals to a usable voltage for the FM modulator. This signal is then added to a synchronization timing signal which will allow the determination of which electrode is producing that particular signal level.

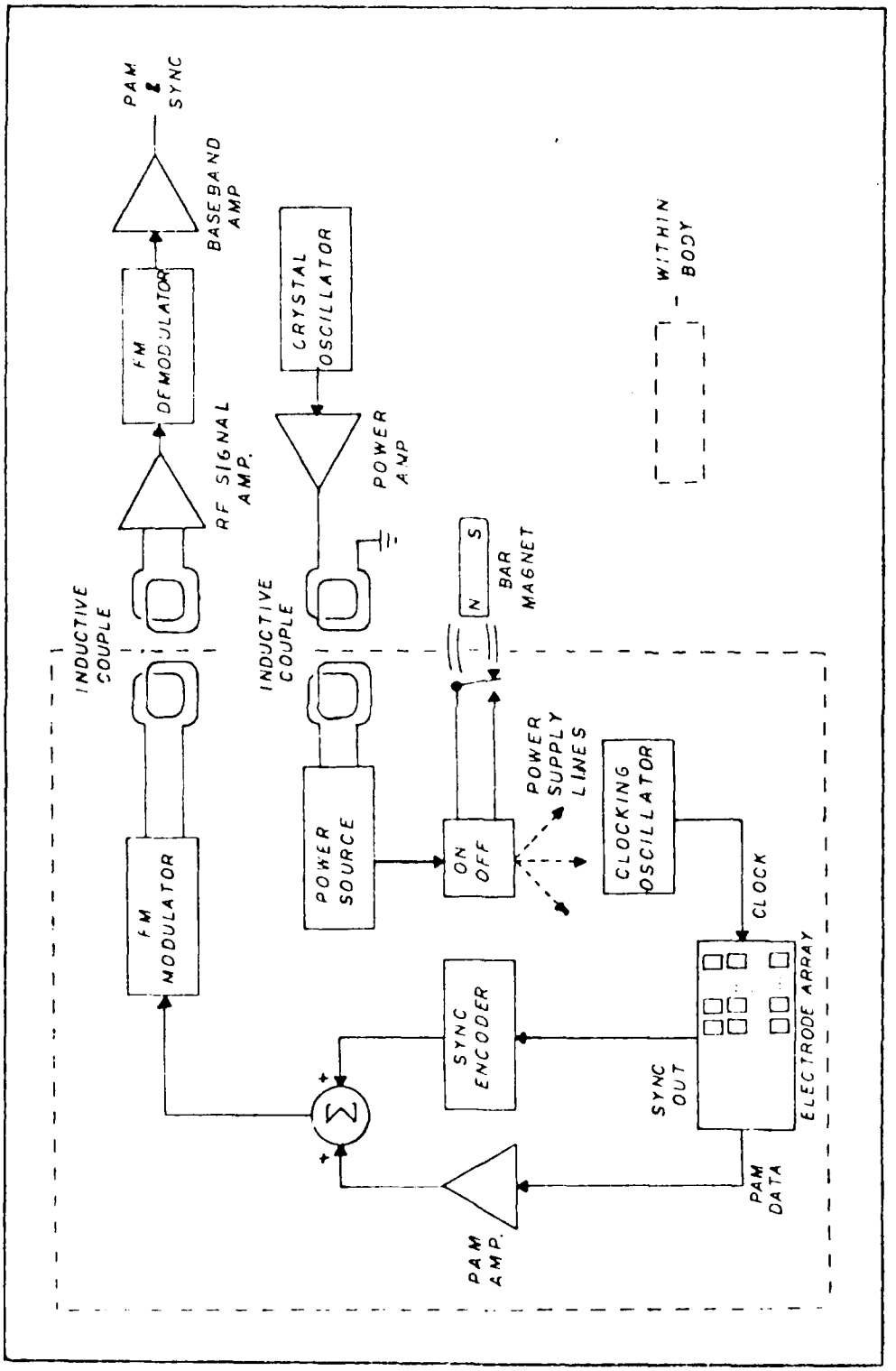


Figure 2.2. System Block Diagram

once the signals are added together, they form the modulating signal for a wideband FM modulator. The FM modulator in turn drives an inductive loop antenna which is inductively coupled to the demodulator. All of the signal processing and modulation is performed within the body cavity and the loop antenna is placed near the surface of the skin to maximize transcutaneous signal level. Outside of the body, a close proximity inductive loop antenna picks up the modulated signal and amplifies it to a level acceptable for the input to FM demodulating phase locked loop. The demodulated signal produced by the phase locked loop is then low pass filtered and amplified to be used as an input to other devices to demultiplex the PAM signal. The demodulator is a separate unit and is in place only when data are collected.

The final functional unit is the power supply and support circuitry (clocking signals and control for the electrode array). This system has both internal and external components. External components include a medium frequency crystal controlled oscillator which is power amplified and matched to a power transmission coil. Power gain is adjustable to meet requirements of battery charging, distance, and efficiency. Internal to the body is a receiving coil completing the inductive couple and power transfer. The incoming power signal is then rectified and smoothed to suitably charge an internal power source. Power transfer and data output will be run at different times to avoid coupling problems, so a on/off switch is provided to

turn on the implanted telemetry and the electrode array.

The following sections develop the system requirements of each one of the blocks in the diagram and present a simplified method for solving each particular design problem.

Internal Circuitry. Each element of the data signal processing and FM modulation circuits has unique requirements placed on them by overall system performance and by interfacing of individual circuits to one another. Each of the following sections describes what system requirements must be met and what requirements are imposed by the design of that stage or of other stages connected to it.

Data Amplification. The amplification of the output data stream from the electrode array is constrained by the source impedance of the electrode, by the gain required to adequately modulate the FM modulator and by ultimate power consumption. Input impedance is of particular importance since a significant amount of voltage can be lost within the lossy source of brain tissue and impedance of the electrode (which varies as the biological event takes place) (17:154). Impedance of electrode to brain tissue interface is dependent on the nature of electric double layer formed when a metal electrode is placed in contact with an electrolyte solution such as the cerebral fluid. This layer behaves like a capacitor shunted by a resistor both of which are frequency and current density sensitive (17:213). The resistance varies from subject to subject and with electrode size and

impedance is about 1 to 50 kilohms. Electrode impedance along with the resistivity due to the actual tissue makes the source impedance quite high in most applications. To avoid distortion from signal attenuation due to resistive losses and the changes in current density when a low impedance amplifier is used, very high input impedance amplifiers must be used to monitor the electrode signal (17:224-233, 240-244). Input impedance of the amplifier must be 10 to 20 times greater than source impedance requiring an input impedance of approximate 500 kilohm or greater. Low bias currents are required to prevent the movement of electrode material into the brain due to electrolysis. In addition, permanent damage to brain tissue can result if current density becomes too high for long recording periods, due to strong current paths set up in the tissue.

Not only must the amplifier have a high input impedance, it must also have a strong immunity from common mode signals on the reference electrode and the monitored electrode. This requirement stems from the large amount of low frequency noise in any environmental set up. Noise sources like AC 60 Hz line power, motor spikes, and background switching circuits cause large amounts of common mode signals to likely be present at electrode surfaces. Common mode noise sources can produce signals well in excess of several millivolts, which is significantly greater than the 20 to 1000 microvolts signals seen at the electrodes. This requires the input

Input of the amplifier must be differential with a common mode rejection ratio of 50 db or greater to achieve good signal representation without significant common mode interference (18:684; 19:218).

Frequency response of the amplifier is determined by the characteristics of the input PAM waveform and the allowable rise-time deterioration of the waveform due to loss of high frequency response. Electroencephalographic signals display a spectrum consisting of primarily low frequencies with an upper frequency limit of 25 hertz. No significant spectral content exists above this 25 hertz limit, making it feasible to take sufficient samples to reconstruct the waveform. Nyquist theorem states the minimum sampling rate must be twice the bandwidth of the baseband signal (20:298).

$$F_{sample} = 2W \tag{2.1}$$

This assumes ideal impulsive sampling and an ideal low pass filter for reconstruction of the waveform. The actual signal, however, is far from ideal because of nonimpulsive sampling (first order sample and hold), signal distortion at electrode interface, band limited communications channel which causes crosstalk between samples, and the use of practical low pass filters for signal reconstruction. The nonideal nature of the system, suggests the signal be sampled at a rate of 3 or 4 times the maximum baseband signal, or in

skin as the dielectric. The skin is a lossy dielectric, strongly frequency dependent, and subject to change upon environment or emotional changes. To pass signals, a common ground between external and internal systems is necessary, and this can only be accomplished through the highly resistive body fluid which is not suitable for high quality transmission.

Consequently an inductive couple was then tried. Because of the high amount of deviation of the carrier, a low Q tuned circuit was needed to avoid detrimental amplitude modulation distortion of the FM modulated signal. However,the low power handling capabilities of the output stage of the CMOS phase locked loop couldn't sufficiently drive a parallel low Q tuned circuit. So, a series tuned output couple was tried where the output center frequency was at the harmonic near 10.7 MHz and component values were chosen so the impedance at the fundamental frequency was high to prevent loading of the PLL. This approach increased the modulation index by number of the harmonic used and because the output of the phase lock loop is a square wave, there is sufficient energy in the side bands to produce a detectable amount of signal in a coil placed near the tuned circuit. However, the tuned circuit rang when driven by the output stage and produced unusable signals for demodulation. Even if the circuitry had worked, the efficiency of the system would not be acceptable for low power applications. The use

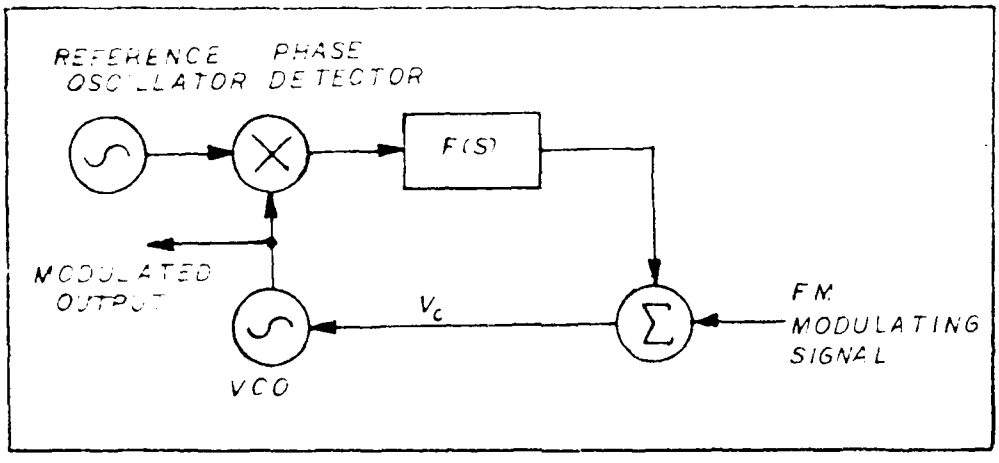


Figure 3.1. Phase Lock FM Modulator

A commercially available CMOS phase locked loop, CD 4046, was chosen and design was undertaken to produce a FM modulator with a 100 to 150 KHz deviation at a frequency of approximately 1 MHz using the voltage controlled portion of the PLL. The design preceded, but it was found that the maximum achievable operating frequency was about 750 Khz with some uncertainty in frequency stability. A phase locked frequency modulator was then tried but exhibited a very low modulation index without the divide by N counter in the feedback loop. Alternatively, the divide by N counter does help some, but forces operation at a harmonic of the reference oscillator requiring a very high stability reference oscillator. Further complicating matters was the problem of transmission through the skin of the modulated signal. Initially coupling was to be capacitive, however capacitance required to pass the signal unattenuated,

changes and problems that occurred will also be discussed.

Internal Circuitry

Overview. As discussed in Chapter II, the primary requirements that must be faced in the design of the internal circuitry are low power, achievable bandwidths, simplicity, and scalability. The purpose of a prototype is to check the feasibility of such a system. The internal circuitry tends to stretch the limits of existing integrated circuits. Achieving large bandwidths at low power is a conflict of terms, especially in the early development of operational amplifiers, μA 709 and μA 741, where power is an easy sacrifice for high gains. Also low level signals are being measured, meaning noise must be minimized- another conflict to low power and large bandwidths. In the following section, the author will look at the design of the outward link of the communications system, taking into consideration these conflicting requirements.

FM Modulator. The FM modulator was the first area of design because it defines the requirements for both the amount of gain required and operating frequency of the demodulator. The first cut at this problem of a low power FM modulator was to use a CMOS phase locked loop and to modulate it while it is locked onto a stable oscillator (see Figure 3.1).

III. Communications Link Design and Breadboarding

Introduction

This chapter deals with the design, breadbroading, and initial performance evaluations. The first section deals with the internal circuitry of the communication link which includes the amplification of the multiplexed pulse amplitude modulated signal, the addition of synchronization information, and the frequency modulation of a radio frequency carrier. The second section deals with the external circuitry of the communications link which includes the front end receiver and amplifier, the FM demodulator, and the baseband output filters. Each section will present a description of the design considerations and governing equations, the processes used to determine a workable solution, and a description of the actual implemented system. In addition, each section will describe the breadboarding of the circuits and the steps taken to realize a workable system in an environment where radio frequency noise and crosstalk make designing, at best, difficult. The order of presentation within each section represents the order used in the actual design to determine the necessary requirements of subsystems, while not causing major redesign of the system when requirements changed or could not be met. By breadboarding in a systematic fashion, the system performance was evaluated and the design was revised to improve the

implantable system, the total system must be able to be implanted within the chest cavity of a rhesus monkey. Approximate size would have to be a maximum of 6 cm by 6 cm by 4 cm in size and capable of being affixed to bone so that movement within the chest area is minimal. The shape must have smooth edges and be sealed so saline body fluids do not penetrate and cause failure in the electronics. Materials used cannot damage surrounding tissue or cause harmful substances to enter the blood stream. This thesis will not perform the actual fabrication of the implantable system, but design considerations are being done with ultimate implantation constraints considered. Miniaturization of circuit designs into thick film circuits of minimal complexity allows size requirements to be met. As available tools increase in the future, chips sets performing all signal processing functions can be placed on site with the electrode array, improving the data transfer. More discussion of size and fabrication will be addressed in Appendix F.

[illegible] must be provided. Implantable rechargable power sources require small size, good power to weight ratios, relatively stable supply voltages, biocompatability (generates no gases or heat), and must be capable of many recharge cycles (25:263-264). Within this system, the power supply must supply 25 mA to the electrode array at 5 volts and approximately 5 mA for the amplifier, RF modulator, sync encoder, and clocking oscillator, for a period of approximately an hour between recharging. Recharging times should be relatively quick to prevent discomfort to the animal and reduce the possibility of equipment damage by the animal. On/Off capabilities must supply voltage upon command by a simple couple through the skin. The switch must not change the applied voltage significantly or interfere with the transmission of the PAM electrode signal.

Clocking Oscillator and Pin Connections. The clocking oscillator and pin connections requirement result from the need to produce the proper conditions for the electrode array to sequence through each electrode. Clocking oscillator must be fairly frequency stable stepping through the array electrodes at a rate of 25 kilohertz. The pin connections must insure that proper values of high and low are seen at count-select and sync-in pins to force the array through the proper sequence. Power supply ground and 5 volts will be used.

interference with other devices and keep the system at optimal performance, the output signal should be a well filtered sinusoid to keep out harmonics which degrade performance.

Inductive Couple. The inductive couple provides an efficient link of energy through unbroken skin. Conductive tissue surrounds the implanted coil forming a lossy magnetic shield to RF signals. Fortunately, the shielding is incomplete and inversely proportional to frequency (23:259-261). This tends to make the antenna (coil) more efficient at higher frequencies causing a trade off in design parameters as discussed in the oscillator section.

To further improve transmission properties, the Q of the circuit must be kept reasonably high, despite the tissue losses. To do this, the reactive component of the inductor or capacitor at resonance must be kept low (approximately 100 ohms) (23:261). Position tolerance of the couple determines how the coil sizes compare. Greater tolerance to misalignment of the coils, results in loss of power transfer efficiency which must be considered in the ultimate design.

Power Source and ON-OFF Switch. The power source must be a rechargable source capable of delivering sufficient power to implanted circuitry. To conserve power and limit the required size of the batteries, an externally

spectral purity for highest efficiency of power transfer. This is so because coupling circuits are tuned to high Q circuits with very narrow bandwidths. Any harmonics produced outside the narrow bands are lost as heat in the output circuits and are not available for powering the device. Frequency of the crystal oscillator is determined by a trade-off of coil efficiency at high frequencies, depth of penetration at low frequencies, and tissue losses at over a range of frequency (23:259). Since depth of penetration is an exponential function of distance, measured in wavelengths from the surface, better coupling can be achieved if low frequencies are used.

Rules and regulations of operating bands of high power transmitters further limit acceptable bands for operation of the transmitter, forcing the use of commercial or amateur bands. In using any frequency, interference with operating devices nearby must be evaluated.

Power Amplifier. The power amplifier's requirements are power amplification, impedance matching, high spectral purity, and high efficiency of power generation. Typical trascutaneous telemetric powering systems have power transfer efficiencies of 6% to 25% depending on coil shape and spacing (24:634, 638). Output power for a usable charging power of 250 milliwatts is in the range of 1 to 5 watts. The output power must be transmitted

critical processing of the signal for both clocking information and signal reconstruction has not been fully categorized. Filtering accomplished in the baseband amplifier extracts the PAM signal from the noisy signal produced by the phase locked loop. The noise is characterised by its frequency content at the frequency of the voltage controlled oscillator and is easily removed. A low pass filter at a cutoff frequency of 150 KHz will provide adequate high frequency suppression and good quality signal extraction. Filtering must not introduce any perceivable overshoot in the step like PAM signal. Edges must be sharp and clean and noise should be limited to that generated by the input amplifier at the electrodes.

Power Supply and Support Circuitry. The power supply for the telemetry link is composed of a crystal controlled oscillator, a power amplifier, rechargable power source, and an on-off switch. Each section of the power supply has requirements of stability and efficient operation in very changeable surroundings. Support circuitry includes the clocking oscillator and sequencing connections. Here the emphasis is on proper operation of the electrode array. In that context, the individual requirements of each block in Figure 2.1 will be described.

Crystal Controlled Oscillator. The crystal controlled oscillator's requirements stem from the need of a highly stable reference frequency at which power transfer

Empirical observations note the use of close proximity coil for coupling reduces gain requirements to around 100. The frequency response must be able to handle incoming RF frequencies while presenting a small output impedance to the FM demodulator.

FM Demodulator. The FM demodulator requirements are to extract the frequency modulated information with the minimum amount of distortion to the transmitted waveform. This requires that the output frequency response bandwidth be 100 KHz. Further, a filter must be used to remove high frequency noise generated by the demodulation process. Because loading and voltage supply changes in the modulator cause shifts in the center frequency, the demodulator must track small changes without retuning of the demodulator. The demodulator should not be sensitive to amplitude changes of the incoming signal that might cause a loss of lock or distortion of the data signal. This is especially important since mistuning of the tuned coil in the input will cause amplitude differences at different frequencies resulting in amplitude modulation at the same frequency as the modulating signal. Due to the characteristics needed, a phase locked loop is the logical choice to achieve a tracking demodulator.

Baseband Amplifier. The baseband amplifier provides two functions to the signal processing of the recovered signal; amplification and filtering. The requirements for amplification cannot be defined since post

detailed [illegible]. The low power transmitter must be stable at the center frequency with a variety of output loadings and under significant changes in supply voltages. The modulator must demonstrate good linearity and be monotonic through out its operating range. A possible technique for FM modulation to produce stable modulation is a crystal referenced low power phase locked loop where the voltage controlled oscillator is directly modulated by the input signal. Another possibility is a simple oscillator design using a voltage controlled variable capacitor (varactor) as part of its tuning tank (22:165-167, 96-100). Design criteria for the FM modulator is low power (less than 5 milliwatt), simplicity of design (low part count), high frequency stability, and compatibility with simple demodulator design.

External Circuitry. The demodulator requirements are related to ease and quality of reproduction of the transmitted PAM signal. Here design requirements are placed on all three segments, RF signal amplifier, FM demodulator, and the baseband amplifier. Each unit should be designed using commonly available integrated circuits and using as simplistic a design as possible. Discrete electronics are a last resort for each stage in the design.

RF Amplifier. The RF amplifier must perform amplification of a low level radio frequency signal to a level suitable for the FM demodulator. The input to the amplifier must be tuned to eliminate out-of-band noise.

Frequency Modulator. The frequency modulator must take the PAM signal from the amplifier and use it to modulate a radio frequency carrier suitable for good FM broadcasting and simplicity in receiving. For a good quality signal, a modulation index in excess of 1 is required. The baseband signal determined in the previous section was approximately 100 KHz, so a modulation deviation 100 KHz is the minimal requirement. This thesis will use a deviation of 150 kilohertz to give somewhat better performance. The modulation index is actually significantly better than 1.5 determined above, since the major contribution to the spectrum is in the range between one half the sampling rate and the sampling rate. This is evident when adjacent electrodes have equal but opposite voltage resulting in a square wave with a frequency of one half the sampling rate. At a sampling rate of 25 KHz, the modulation index is 12 which falls well into wide band FM and its associated noise improvement over other modulation techniques.

The frequency modulator's center frequency will be determined by the ease of demodulation. Frequency bands for biomedical research are 38-41 MHz, 88-100 MHz and 174-216 MHz with maximum signal strengths of 10, 50, and 150 microvolts per meter at 15 meters respectively (21:21). These bands are for higher power telemetry units; lower power telemetry is open for most other bands so long as power levels at 15 meters are undetectable. Close proximity inductive coupling coils reduce the required output power, and simplify

analysis, the relation between bandwidth and RC time constant is given by equation 2.2.

$$\tau = RC = 1/2\pi B \qquad (2.2)$$

Substituting in the required period, the bandwidth required is approximately 100 KHz for good to excellent reconstruction of the step edges. Although the analysis appears very conservative, other effects like charging of the electrode's shunt capacitance causes the combination of effects to result in degradation of a stabilized value within one fifth of a period.

Amplification of the signal must be sufficient to produce maximum deviation of the frequency modulator. This amplification must also be sufficient to drive the load presented by the input of the modulator. Actual specifications for the modulator cannot be determined until actually implemented, but required voltages are in the range of one volt based on typical varactor specifications. With full deviation being a 1000 microvolt signal, the gain required is approximately 1000. This gain must be relatively noise free so a signal change of 20 to 50 microvolts between electrodes can be detected. With this high gain, frequency response and slew rate of the amplifier become significant however, designs should favor frequency limitations over slew rate limitations.

this case approximately 75 to 100 samples per second per electrode. For the 256 electrode array, this produces a 19 to 25 kilohertz sampling rate. At 25 kilohertz the time period is 40 microsecond between changes of electrode. This results in the stair case type signal depicted in Figure 2-2.

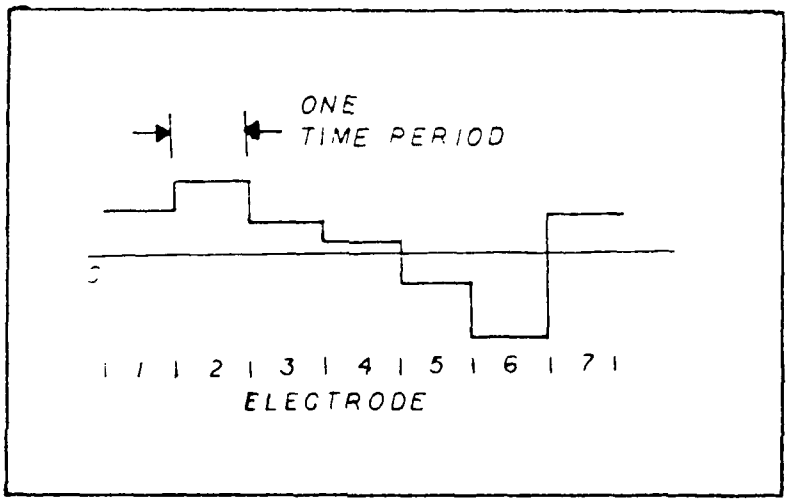


Figure 2.2. PAM Signal

Since each step is very much similar to on/off switching of a DC voltage in a RC circuit, the low pass bandwidth of the amplifier must be sufficient to produce a steady signal within about the first fifth of the period between electrodes. For most engineering work, a signal has stabilized in a RC exponential circuit in 5 RC time constants. Therefore, the baseband amplifier must have a low pass filter with RC equivalent of 1/25 of the 40 microsecond electrode period or 1.6 microseconds. From linear systems

of a phase locked FM modulator was left as impractical until a suitable low power phase locked loop is available that will run in the 10-20 MHz range, so a higher Q parallel tuned output stage can use the fundamental frequency. National Semiconductor has released preliminary information of a CMOS phase lock loop, MH54HC4046, with a maximum frequency of 20 MHz and would be ideal for this application.

Unable to find a low power voltage controlled oscillator in a IC package, the design turned to discrete components in a configuration commonly used in low power applications, a common base Colpitts oscillator using a varactor to produce changes in the center frequency (25:208-209; 26:265-273, 331). Common base configuration was used because of high stability and small center frequency variation over changing supply voltages. Figure 3.2 shows the circuit used in this design.

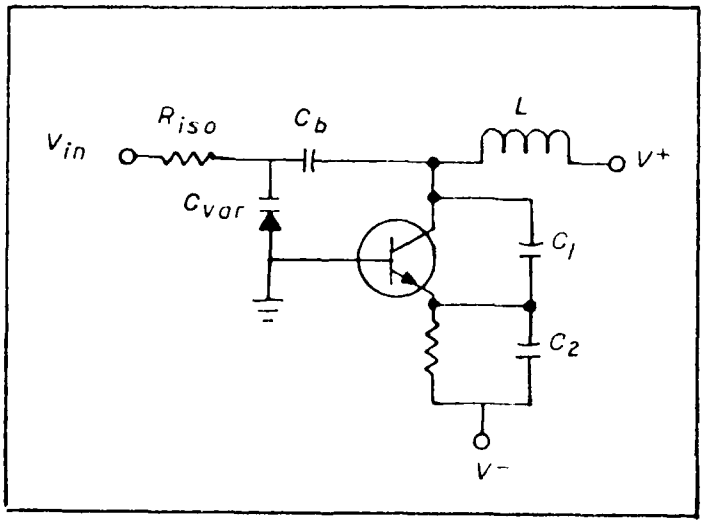


Figure 3.2. Common Base Colpitts Oscillator

Design was undertaken for an oscillator at 9 MHz so the 150 KHz modulation was 1% to 2% of the center frequency, as required by the phase locked loop used for the demodulator. The preliminary design used equations from Haywood's text.but, due to their complexity, they are not presented here (26:267). Preliminary designs did not produce the optimum design when modulation was applied. Changes of operating point due to changes in the varactor's loading of the tank caused severe amplitude modulation as frequency was swept. Nonlinearities in the limiting process, as well as loading of the tank by the varactor, produced the unwanted amplitude changes and forced a trial and error approach for a stable, clean FM modulator (27:368, 370-371). Using approximately a 3 microhenry inductor, 6 1/4 turns on a 3 cm diameter form flat wound, keeps the center frequency inductive reactance at about 150 ohms to maintain reasonable Q despite tissue losses. The choice of varactor was made to produce a 5% change of capacitance when varied in parallel with the net capacitance in the feedback voltage divider C_1 and C_2. Using equation 3.1 to solve for the total required capacitance, we find approximately 100 picofarads needed to produce a 9 MHz carrier.

$$F = 1/2\,\pi\,(LC_{total})^{1/2}, \tag{3.1}$$

Where

$$C_{total} = (C_b C_{var}/C_b+C_{var}) + (C_1 C_2/C_1+C_2) + C_{stray}$$

If the blocking capacitor is kept relatively large, the capacitance variation of the varactor will almost totally be the change of the total tuning capacitance. To achieve a 5% total change of frequency, a change of 5 picofarads at the varactor's bias point is needed. The choice of the varactor MV209 satisfies this requirement and keeps the Q of the circuit high.

Initial trials for proper feedback network used a large DC blocking capacitor, C_b, and a sizable isolation resistance, R_{iso}, to isolate the modulator from a 1 volt p-p signal with 1 volt DC offset provided by a signal generator. Low frequency modulation was used, and the waveform at the collector was monitored for amplitude shifting as the modulator was swept through frequency. Trial and error methods then produced a feedback capacitor pair which generated the least amplitude modulation. Using a sinusoidal modulating signal the approximate 3 db rolloff point for the varactor input was found. The combination of adjusting C_b and R_{iso} raised the cutoff frequency to approximately 150 KHz. Using a lower frequency square wave modulation signal, the feedback network was readjusted for minimal amplitude shift with frequency. The resulting modulator with values determined is shown in Figure A.1 in Appendix A. It should be noted that the breadboarded design depicted in Figure A.1 has total capacitance considerably less than calculated from frequency. Stray capacitance in the windings of the

inductor, in the junctions of the transistors, and in circuit wiring forces a design where trial and error are used to produce optimum results. Likewise the cutoff frequency for input modulation appears low, however, Miller capacitance generated across the base to collector junction significantly adds to the low pass filtering effects of the varactor network. To provide a good high frequency current loop for the output oscillator, 10 to 15 microfarad bypass capacitors should be placed between the supply lines and ground, physically close to the modulator.

Before any other design could be accomplished, a plot of frequency verses applied voltage was taken. This plot is shown in Figure 3.3. The curve is very nonlinear, especially in the extremes of the operating range. The most linear region of the curve will be used as the operating range of the modulation, determining the DC operating point and required voltage swing. This defines the gain needed to produce full modulation for the full scale input of 1 millivolt peak to peak. The most linear region of the graph is the region between 8.8 MHz and 9.1 MHz requiring a .9 volt swing centered at 1.3 volts. The present application does not force the transfer relation to be linear, so long as it is monotonic and characterizable so an inverse relation for compensation can be determined, if needed. Absolute voltages on the surface of the brain are not the measure of importance, but rather the relative changes between electrodes normalized over the maximum absolute value.

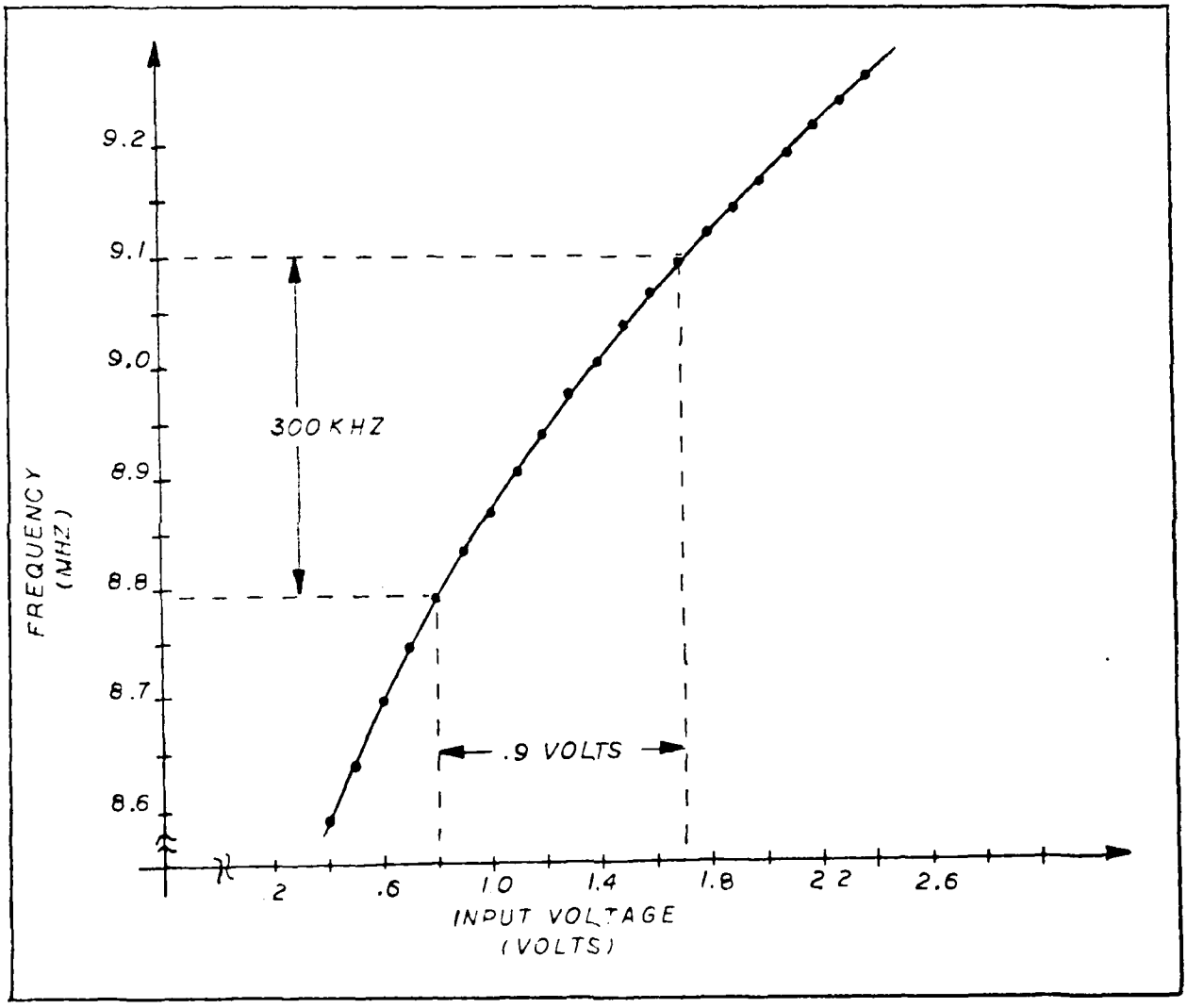


Figure 3.3. Modulator Characteristics

3.3 Amplifier. The design of the amplifier for amplifying the electrode signal to a useable level for the modulator must take into account a lot of conflicting requirements. Requirements of high bandwidth (100 KHz), low power (under 20 microwatts), high slew rates, low noise, and high common mode rejection ratio all contribute to a very specialized design where many tradeoffs must be made to fulfill a practical design. The first task was to find a suitable amplifier to produce the needed amplification. Amplification of 900 to 1000 is needed to produce full modulation with the maximum input voltage of 1 millivolt, forcing the amplifiers to have at least 80 db of isolation between stages. The amplification should be performed over no more than 3 to 4 stages to avoid self oscillation from currents setup in the feedback networks. The minimum exceptable gain-bandwidth product of a single stage is 600 KHz, but to avoid any significant losses at higher frequencies, a better figure is 850 KHz. The final amplification stage must be capable of a slew rate of .9 volts in 1.6 microseconds, one fifth of the time between electrode samples, or 0.5625 volts per microsecond. This must be done at low voltages since a maximum of 5 volts is available between positive and negative supplies and the amplifiers must remain immune to changes in gain when supply voltage varies. Two commercially available amplifiers are capable of such characteristics, the LM 146 programmable operational amplifier and the LM 158/258/358 family of low

four operational amplifiers. The choice of LM 146 for the first stages of the amplifier was made because of lower noise specifications for the unit (see Appendix D for data for particular devices).

To achieve the very high input impedance required for the monitoring of a high source resistance brain signal, a differential input is required. Standard inverting or noninverting amplifiers using simple voltage divider feedback connections reduce input impedances below the source impedance. Furthermore, a change in feedback to increase the input impedance causes a reduction of gain certainty, effectively reducing the common mode rejection ratio (CMRR) (19:218). The solution to the problem is the compound differential amplifier known as an instrumentation amplifier. As seen in Figure 3.4, the amplifier is composed of 2 noninverting amplifiers commonly connected through a floating ground.

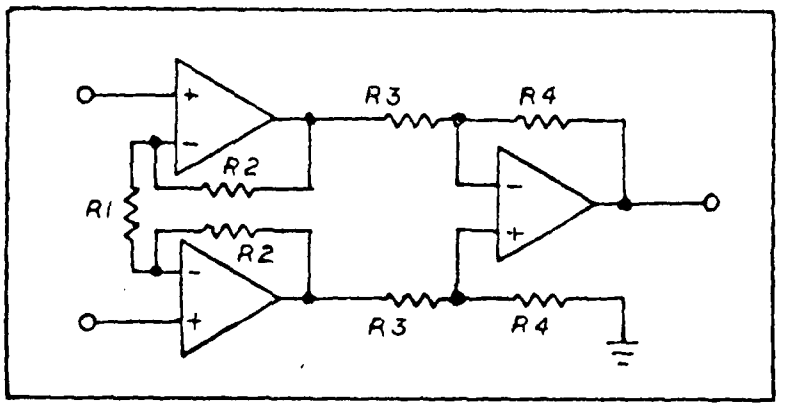


Figure 3.4. Instrumentation Amplifier

These are used as inputs to a difference amplifier which provides the common mode rejection. The problem with this circuit is that to achieve the highest possible common mode rejection, the gain of the input amplifiers and of each leg of the difference amplifier must be exactly equal. Because of the floating ground arrangement of R1, the common mode gain of each of the first amplifiers is unity and the difference amplifier produces the required CMRR for the system. To provide as equal gains as possible, resistor values for R2, R3, and R4 must be 1% values.

Design was accomplished so the first set of amplifiers has a 3 db cutoff point near the required 100 KHz. Some top end room was left for expandability and rolloff. The gain for the first stage is given by equation 3.2.

$$A = (1+2(R2/R1)) \qquad (3.2)$$

Fairly low resistances were used in the first stage to improve gain certainty and reduce the effects of resistor noise in the total noise of the amplifier. A gain of 21 was chosen for the first stage and was implemented with R1 = 6.8 kilohms and R2 = 68 kilohms. Each amplifier provides a gain of approximately 10.5. For a bandwidth of 150 KHz, the required gain-bandwidth product was 1.6 MHz. From the tables in the data sheets for the LM146 (see Appendix D), the required I_{set} is 20 microamps at the lowest exceptable operating voltage of 4 volts. This requires a 68 kilohm

[illegible] The second stage gain is 8 and has larger bandwidth to avoid a double pole of the corner frequency. Matched sets of resistors with values of R3 = 22 kilohms and R4 = 180 kilohms achieve the gain of 8 using equation 3.3.

$$A = R4/R3 \tag{3.3}$$

The large bandwidth does not introduce any significant noise since front end noise is already 20 times greater than any contribution in the second stage. Finally a third stage (not shown) completes the amplification using a common inverting amp with a gain of 5.6. Here no special resistors are needed and the gain is achieved by an input resistor of 100 kilohms and a feedback resistor of 560 kilohms.

Breadboarding of the design requires adherence to good symmetry. Layout of wiring paths and resistor placement should be equidistant from onboard noise sources like oscillators and switches. Also differential inputs should be a twisted pair of wires all the way to the electrode array, so that any coupled external noise is exactly the same in each line. This way the common mode rejection of the amplifier will remove any unwanted noise. Other precautions are to keep smoothing capacitors on the supply lines physically near the amplifier to help suppress switching transients caused by CMOS gate switching. Great care should be taken to make sure symmetry and matching are well adhered

mode noise.

Synchronization Encoder. The synchronization encoder's design objective is to place a readily distinguishable mark in the waveform to give the recorder the knowledge of where in the array each particular voltage came from. To accomplish this marking, a sync pulse from the electrode array must be high for only 1 time period when a single electrode is on. The AFIT electrode array provides such a signal when the 256th electrode is turned on signifying the end of the count and the return to electrode #1. The encoded mark must be separable from the samples taken by the electrodes and not be corrupted by the signal present on the 256th electrode. To accomplish such a mark, a simple voltage level greater than any produced by the electrodes will take the place of the level on the 256th electrode. A switching network (see Figure 3.5) made of 2 analog switches from a CMOS CD 4066 provides a means of placing the multiplexed PAM output of the electrode array on the line when the sync level is low and placing the voltage marker on the line when the sync level is high. To create a reference voltage for the marker, a single forwardly biased 1N914 diode was used. This was used to provide a fairly stable voltage reference while supply varies from 5.5 to 4 volts. Low power is achieved by use of a 82 kilohm biasing resistor.

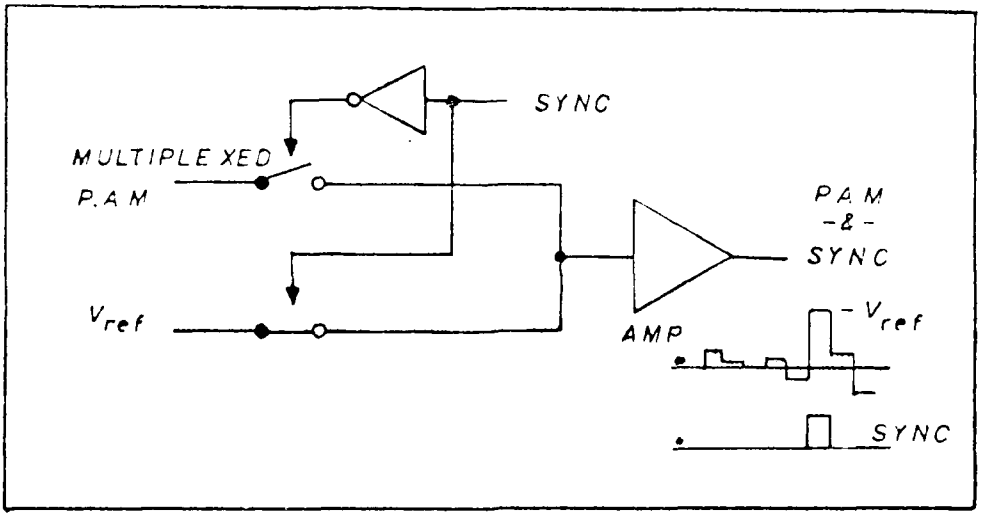


Figure 3.5. Synchronization Encoder

This approach was used over a Zener diode because of low power and a non critical bias point.

From test results taken on the diode used, a 82 kilohms bias resistor produces a 0.216 volt reference which varies no more than four one hundreds of a volt over the projected supply range and uses a maximum current of 30 microamps. The reference voltage needs to be approximatetly 0.6 volts to produce a level significantly larger than that applied by the electrode signal. A summing amplifier (LM 358) multiples the references voltage by 3 when selected by the switching network and the multiplex electrode signal passes through unmodified when selected. The complete system can be seen in Figure A.1 in the Appendix A.

Internal System Interconnection. Each section of the internal system design is connected by capacitive coupling. To prevent significant tilting of output waveforms, the capacitive value must be fairly high. DC blocking is necessary because signal voltage levels at the sync encoder network need to be added from the same ground reference point. Capacitive coupling between the encoder and FM modulator is needed to set the DC bias which must be added to the modulator input to achieve the most linear modulation point. The required DC bias is produced by a voltage divider made from a potentiometer connected across the 5 volt supply. As the supply varies so does the operating point causing reduction of the linearity of the modulator characteristics. However, so long as the signal remains reasonably monotonic the data taken under nonoptimal conditions are usable.

External Circuitry

Overview. The external circuitry of the communication link is a receiver using integrated circuits to provide front end amplification, phase locked demodulation, and baseband filtering and amplification for further processing. The following sections will describe the system's designs, and the procedure taken for making a usable breadbroaded receiver. As in the internal system, the order of development in this section will be the order in which the design was undertaken.

Phase Locked Loop Demodulator. The design of a demodulator was undertaken knowing the design of the internal modulation system. The first objective when designing the modulator was to keep the carrier frequency in a range which could be easily demodulated by a phase locked loop. Changing supply voltages over the operating period of the modulator and variable resonance points for different loadings of the output transmitter coil force the demodulator to track slow variations of center frequency without degradation of the received signal. The best solution is the phase locked loop depicted in Figure 3.6.

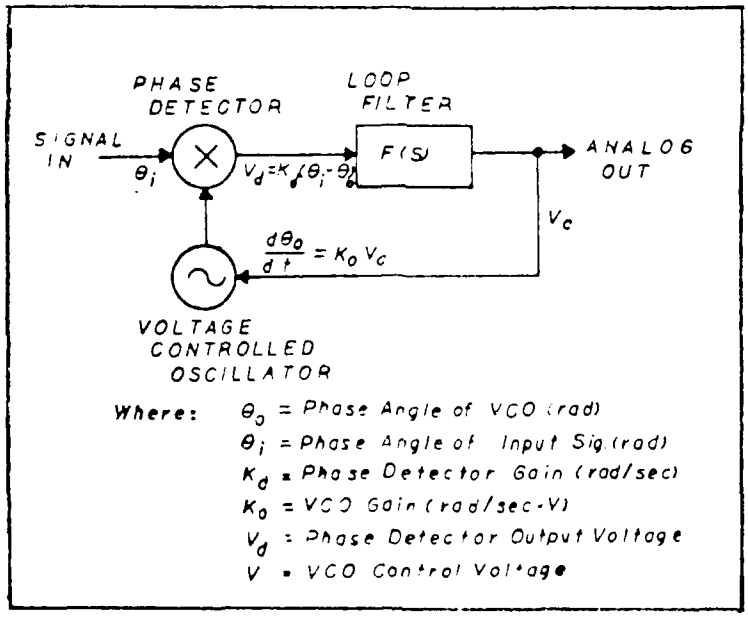


Figure 3.6. PLL Demodulator

The principles of phase locked loops are well known and will only be generalized here to aid in the understanding of the design procedure taken (22;28).

[illegible] The [illegible] of operation of the phase locked loop has its foundations firmly implanted in feedback and control theory. As depicted in Figure 3.6, the phase locked loop is composed of a linear phase detector, a low pass filtering network, and voltage controlled oscillator whose frequency is controlled by an external voltage. The phase detector compares the phase of the periodic input to the phase of the output of a voltage controlled oscillator producing an output voltage proportional to the phase difference. This voltage is then lowpass filtered by the loop filter to produce a low frequency control voltage to be applied to the VCO. The control voltage shifts the operating point of the oscillator in the direction which reduces the difference in phase. When the loop is in lock, the changing frequency of the FM modulated carrier is tracked as the loop attempts to produce a constant phase error. The ability to capture and track a modulated signal is a function of the loop filter design. For slowly changing modulation, only a small amount of information is extracted by the low pass filter, requiring a low bandwidth filter. As frequency of the modulating signal goes up, the information content as well as the bandwidth of the low pass filtering network goes up. Filter parameters must be tuned to handle fast transients, otherwise high frequency components may be attenuated or delayed. The overall functional relationship of the response is a function of the loop gains K_p, the gain of voltage due to the difference in phase, and K_o, the gain

Nickel-cadmium batteries provide a reasonable solution to the rechargable power supply problem. The batteries have a good power density and the best cycling characteristics of the available cells. Because the technology has existed since the middle nineteen sixties, developments well suited to the implanted system have emerged. Nickel cadmium cells have been hermetically sealed with any internally created gases forced to recombine within the cell. Fast charging cells allow quick turnaround times (at least better than earlier cells with 12 to 24 hour rates) and do not heat excessively when over-charged at fast charging rates. Toxic gas retention and cool operation keep the implanted power supply compatible with the surrounding tissue.

Radio frequency powering transmitter consideration comes from the need for efficient safe power transfers to the rechargable cells. The skin and other body tissues present a very lossy dielectric around the implanted coil and between the coils forming the inductive couple. Because body tissue is conductive, a skin effect exists where signal strength exponentially decays with distance measured in wavelengths of the RF signal. This means the implanted coil should be as near to the surface as possible and lower frequencies provide better penetration. However, implanted coils operate more efficiently at higher frequencies, making for a tradeoff of depth of implanted coil versus frequency of operation.

Coil size and shape consideration also play a significant role in the design of radio frequency power

Common name	Nickel-cadmium (sealed)	Silver-cadmium	Lead-acid	Silver-zinc	Lithium* Titanium Disulfide
Electrochemical system	Nickel-cadmium	Silver-cadmium	Lead acid	Silver zinc	Lithium
Voltage/cell	1.2	1.1	2	1.5-2.1	1.5-1.9
Negative electrode (anode)	Cadmium	Silver oxide	Lead calcium/antimony	Silver zinc	Lithium
Positive electrode (cathode)	Nickel-hydroxide	Cadmium oxide	Lead dioxide	Zinc	Titanium disulfide
Electrolyte	Aqueous solution of potassium hydroxide	Potassium hydroxide	Gelled solution of sulphuric acid	Potassium hydroxide	–
Cycle life	300 to 2000	150 to 300	200 to 400	25 to 100	–
Typical capacities	20 mAh to 10 Ah	100 mAh to > 50 Ah	30 mAh to 25 Ah	50 mAh to > 50 Ah	70-90 mAh
Energy density					
W h/kg	26-35	48-75	17.5-22	88-110	22-26
W h/cm^3	0.079-0.103	0.091-0.165	0.067	0.153-0.195	0.085
Temperature range:					
Storage	-40-140°F	-85-165°F	-40-100°F	-85-165°F	–
Discharge	-40-140°F	-10-165°F	-76-140°F	-10-165°F	–
Charge	32-113°F	32-115°F	32-113°F	32-115°F	–
Shelf life	Fair	Fair to good	Good	Fair to good	Good
Cost:					
Initial	Medium to high	High	Low	High	–

*Preliminary spec. for Battery Division, Exxon Ent. Somerville, NJ, U.S.A.

Table 4.1. Secondary Cell Characteristics

displaying good to excellent voltage stability over most of the operating range and high energy densities. However, cyclability, a key to long term implantation, fails with these cells. Also the high purchase cost and lack of availability make the silver base cell impractical for implantable systems. Inexpensive lead-acid batteries look promising at first, but low energy density and the possibility of leakage of the very toxic gelled sulfuric acid into the tissue, remove lead-acid cells from consideration.

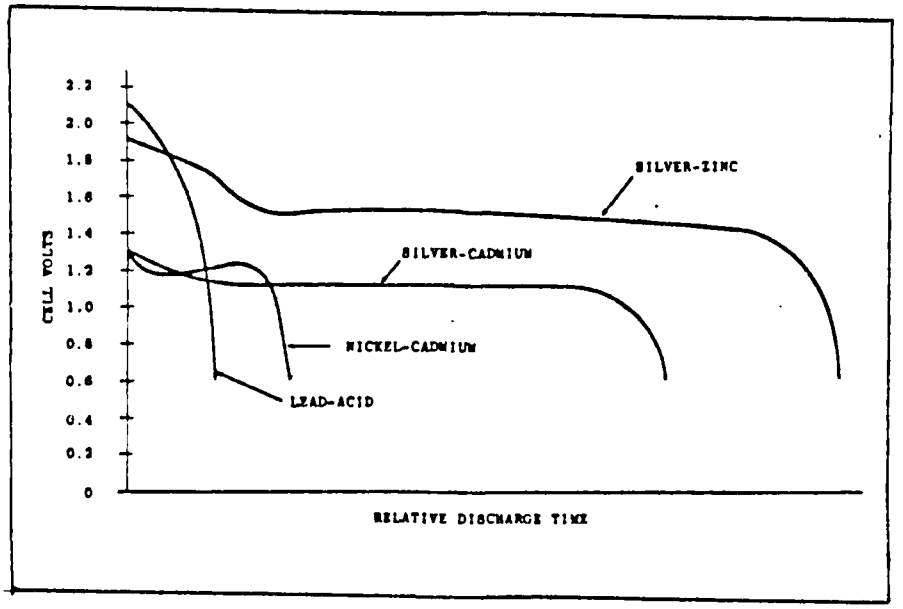


Figure 4.1. Secondary Cells Discharge

To accomplish recharging, a radio frequency transmitter is employed. The characteristics of the powering link are:

1. High efficiency.
2. Spectrally pure transmission frequency.
3. Transcutaneous power transfer using inductive coils.
4. Capable of delivering 250 milliwatts of power through the skin.
5. Adjustable charging rates.

The following section will describe the choices considered for this design and then present the design.

Design Considerations. Designing a suitable power supply for an implanted system requires the evaluation of presently available power sources and recharging systems. Rechargable or secondary type batteries where chosen over nonrechargable batteries or primary type because of the inherent advantages for long term implantability and higher current supply for short periods of time. This does not come without some difficult disadvantages, such as lower power densities, unsteady voltage characteristics, and an awkward charging apparatus. Presently available rechargable cells include lead-acid, nickel-cadmium, silver-cadmium, silver-zinc and experimental lithiums whose discharge curves and characteristics are shown Figure 4.1 and Table 4.1 (31-233, 234). Silver-zinc and silver-cadmium cells would appear to be the optimal choices for telemetry systems,

IV. Power Supply and Support Circuitry

Introduction

This chapter will describe the design of the power supply and necessary support circuitry to keep the transmitter and the electrode array functioning. The two areas covered are the powering supply for the implanted system and the clocking oscillator necessary to step the array through each electrode position. The designs will be discussed first by what considerations were required to produce the design and second, what are the details of the design and how they came about.

Power Supply

Overview. As mentioned in the detailed analysis section (Chapter II), the powering source has some very rigid requirements. The power source must be:

1. Rechargable over many cycles.
2. Stable in voltage.
3. Able to supply approximately 35 mA of current at 5 volts.
4. Externally switchable.
5. Operate at rated current for at least 1 hour.
6. Compact
7. Biologically compatible

proximity to the amplifier chip. These smoothing capacitors help remove parasitic high frequency noise from the ground connection and give clean outputs of the broadcasted signal. The complete design is shown in Appendix A.

The final stage is a 2nd order butterworth active filter depicted in Figure 3.9 (30:169-170).

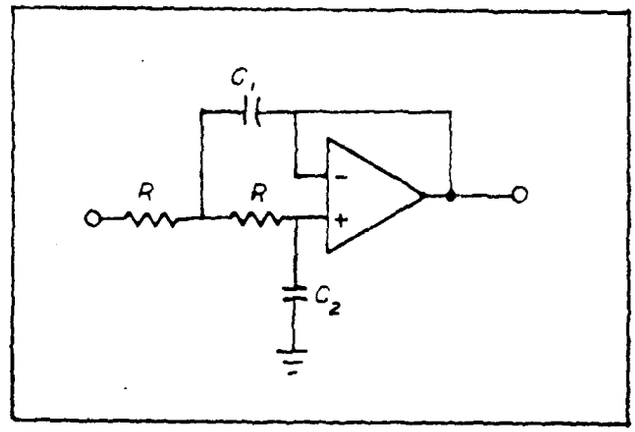


Figure 3.9 2nd Order Butterworth

The filter's cutoff is at 150 KHz and has a dampening coefficient of .7071. Using the design equation seen in equation 3.6 and 3.7 and choosing C2 to be 220 pf, the required resistance is 3.3 kilohms and C1 is 470 pf (29:235).

$$R = (\zeta / w_o)/C_2 \tag{3.6}$$

$$C_1 = (1/\zeta)^2/C_2 \tag{3.7}$$

The filter demonstrates good stability and linear phase throughout the baseband causing no distortion in the waveform. The final output is clean with only a slight high frequency component due to ground fluctuations. In breadboarding, 10 microfarad capacitors were placed from the positive and negative supply lines to ground in close

DC retrieval section of the phase locked loop. This produces large amounts of high frequency noise superimposed on the desired output waveform causing the necessity of several additional levels of low pass filtering.

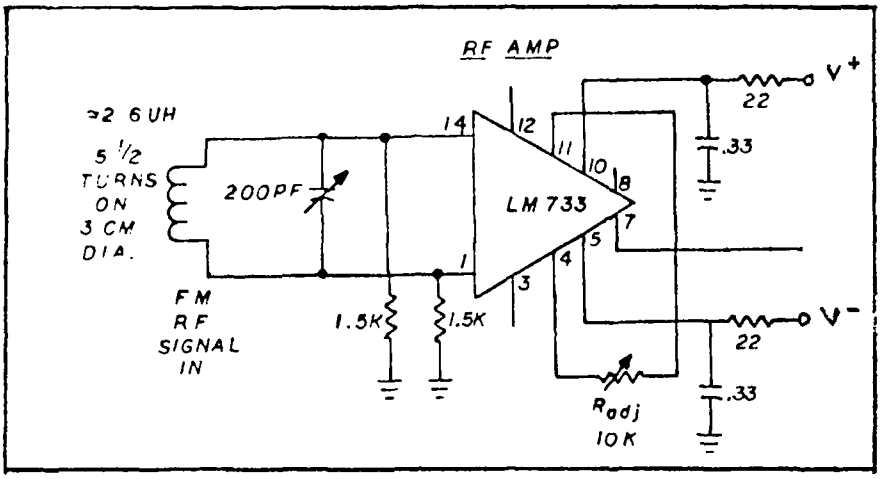


Figure 3.8 RF Amplifier

The filter arrangement incorporates 3 levels of active filtering using a low voltage quad operational amplifier, LM 324. The first stage of amplification provides a gain of only 2 and low pass filtering at 500 KHz due to the limited frequency response of the op amp. High frequency noise still corrupts the signal because the amplifier's feedback network allows some high frequency to pass through. The second stage of the baseband filtering is an unity gain amplifier producing filtering action due to its limited frequency response. This removes more of the high frequency noise but some is still detectable.

controlled oscillator of the PLL. To minimize the problem, decoupling from the power supply was accomplished using a low pass filter of a 22 ohm resistor and a .33 microfarad capacitor taken to ground on both the plus and minus supplies. This significantly helps the problem but additional smoothing capacitors of 10 microfarad between ground and each supply line had to be used to eliminate the interference to controllable levels. Even with elaborate decoupling techniques, long signal lines are sufficient antennae to couple in significant voltage. Keeping the signal path of the amplified RF input to the PLL short, greatly improves tracking and distortion levels. Maximum distance between internal transmitter coil and an external receiver coil is limited not by the received signal level but rather the amount of noise generated by the voltage controlled oscillator of the demodulator. If a larger separation distance of the coils is required, simple cascading of 2 or more LM 733s will provide sufficient gain to amplify a signal into the 100 microvolt plus region. The complete RF amplifier is shown in Figure 3.8.

Baseband Amplifier and Filtering. The baseband amplifier and filters provide high frequency noise removal from the analog signal output of the phase locked loop. Because of the high bandwidth required for good reproduction of the staircase-like electrode signal, it is necessary to use a low value of capacitance for the lowpass filter in the

input voltage of [illegible] when the input coil is 1.0 cm away from the modulator coil, a gain of 5 is sufficient to produce reliable results.

The design of the input coils and tuned circuits are consistent with the objective of reduced losses by keeping the inductive reactance at resonance relatively low. However, because the coil is totally surrounded by air, and eddy current losses in the tissue only occur at close spacings, the Q of this tuned circuit is relatively high. To avoid non linear distortion of the modulated signal over the signal bandwidth of approximately 500 KHz, a low Q circuit is necessary to prevent frequency dependent amplitude attenuation away from the center frequency. An unloaded Q of the circuit should be approximately 20 to allow operation at a distance greater than 1 or 2 inches where coupling is weak and there is little loading of the tuned circuit. To achieve such a Q, the input impedance is effectively formed by the input biasing resistors to ground of the LM 733. To produce an unloaded Q of 20, the required resistance in parallel with the tuned circuit is about 3000 ohms so the bias resistors should be 1500 ohms apiece. To tune the coupling coil, a capacitance of approximately 150 pf is required. A 200 pf variable capacitor provides sufficient range for tuning of optimum center frequency as the center frequency shifts with loading.

Breadboarding of the design once again demonstrated difficulties due to high frequency coupling to the voltage

it is highly preferable to operate from the V+. The internal resistance of the unit was high, making the cutoff frequency fairly low for a small output capacitance to V-. A 470 picofarad capacitor from pin 14 to V- provides some low pass filtering but the 9 MHz carrier frequency dominates the signal, requiring additional low pass filtering. This will be discussed further in the baseband amplifier section of this chapter.

RF Amplifier. The radio frequency amplifier which precedes the demodulator circuitry, provides amplification of the modulated carrier to a level where the widest possible locking range is achieved. From the chart in the data sheets of NE 564 (Appendix D), it can be seen that the lock range begins to fall off at the 100 millivolt range. Because the coil spacing will vary depending on application and positioning of the receiver coil, a variable gain front end is required. The higher frequency requirements of a 9 MHz carrier and the need for high, stable gain leads to the choice of the LM 733 video amplifier to provide initial amplification. The gain of a single differential output can be varied from 5 to 100 by varying a simple external resistor in the feedback loop of the amplifier (see figure 3.8). The LM 733 amplifier is rated at higher gains, however the use of only one of the differential outputs and an operating voltage less than that used for the specifications cause total available gain to be reduced by a factor of 4. With typical

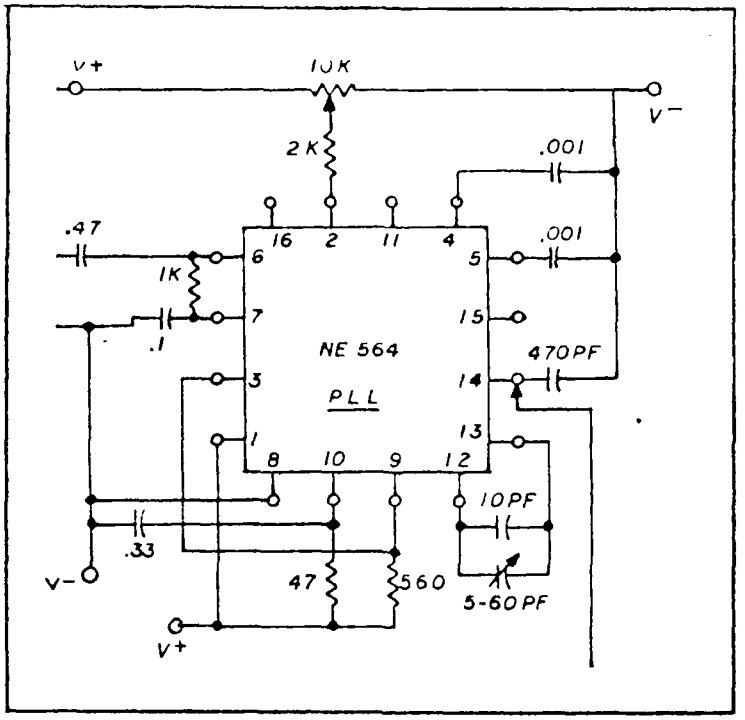


Figure 3.7. FM PLL Demodulator

Also to achieve good modulation, the 10 kilohm potentiometer must be adjusted so the gain is sufficient to provide tracking and dampening of the loop is such that the square wave response has no ringing (see Appendix C for the adjustment procedure). Also the choice of a 560 ohm pull up the resistor for the TTL output of the VCO was to eliminate amplitude modulation effects seen when the VCO was swept between frequencies. Amplitude differences bled into the demodulated signal causing distortion. Another problem in breadboarding results from the recovery of the modulated signal at the analog output. The DC extractor circuit of the

frequency of the input signal (24:1-8). A signal with a 100 KHz bandwidth requires a maximum capacitance of 1000 picofarad for signal reconstruction and tracking. A somewhat smaller capacitors will provide better lock range at the expense of extra noise in the received signal. This simple low pass filter is sufficient for the needs of this application. However, if a bursty or ramp frequency modulation is used, a second order lead lag filter will provide additional control over dampening rates and natural frequency responses of the system. Using the 1000 pf capacitor produced good results but required a high bias current (variable gain control on pin 2) to achieve good results from the demodulator. A complete circuit diagram is shown in Figure 3.7.

Breadboarding the design proved to difficult because of the high frequency and high current of the device. Power supply decoupling was a necessity because high current transients caused by the VCO's 3 volt p-p signal into a 560 ohm load interfered with the input signal and the reference ground of the loop filter. This decoupling was accomplished with a low pass filter composed of a 47 ohm resistor and a .33 microfarad capacitor attached to V- (reference ground for the phase lock loop) in the supply line to the PLL.

of frequency for an applied voltage, which determines how wide a capture and lock range the PLL will have.

PLL Design. The choice of phase lock loop was determined by availability and performance. A Signitics NE 564 phase lock loop was chosen for this application because of its high operating frequency characteristics. Low loop gains did prove to be a hindrance in design and will be addressed here and in Chapter V. Referring to the data sheet (see Appendix D), the capacitance (C), in farads, required for a given center frequency (F_o), in hertz, is given by equation 3.4.

$$C = 1/2500\ F_o \tag{3.4}$$

For 9 MHz, approximately 44 picofarads is required and is implemented with a 10 picofarad capacitor in parallel to a variable 5 - 60 picofarad capacitor.

Implementation of the loop filter is done by capacitors at pins 4 and 5 to ground, with two poles in the loop given by equation 3.5.

$$w = 1/RC \tag{3.5}$$

where

R = 1.3 kilohms (internal)

The low pass filtering performed by the capacitors should be sufficiently wide to encompass the highest modulating

transmitters. Because the coils are air wound and separated, magnetic lines of force are not as ideally coupled as in iron core transformers. This nonideal coupling forces consideration of distance tolerances, and misalignment tolerances in the design of the coils. These problems in the design are treated in depth in the literature (32:612-627; 33:634-640; 34:177-186; 35:177-183). The key points to design are good impedance matching of the load, optimal coil spacing, relative diameters of transmitting and receiving coils, and frequency of operation. Due to the tuned nature of the designs, high Q circuits and good spectral purity makes for more efficient designs.

Powering System and On/Off Switch. In reviewing the literature, a radio frequency powering system designed by Dr. Dean C. Jeutter of Marquette University, showed direct applicability to the design problem presented in this thesis (36:314-318). In order to keep design times reasonable and produce a functional system within the time of this thesis work, Dr. Jeutter's design was used. Some modifications were necessary to produce a working design, however, the transmitter was reproducible and produced excellent results. The modified system shown in Figure 4.2 and Figure 4.3, represents a very close adherence to the design in the literature.

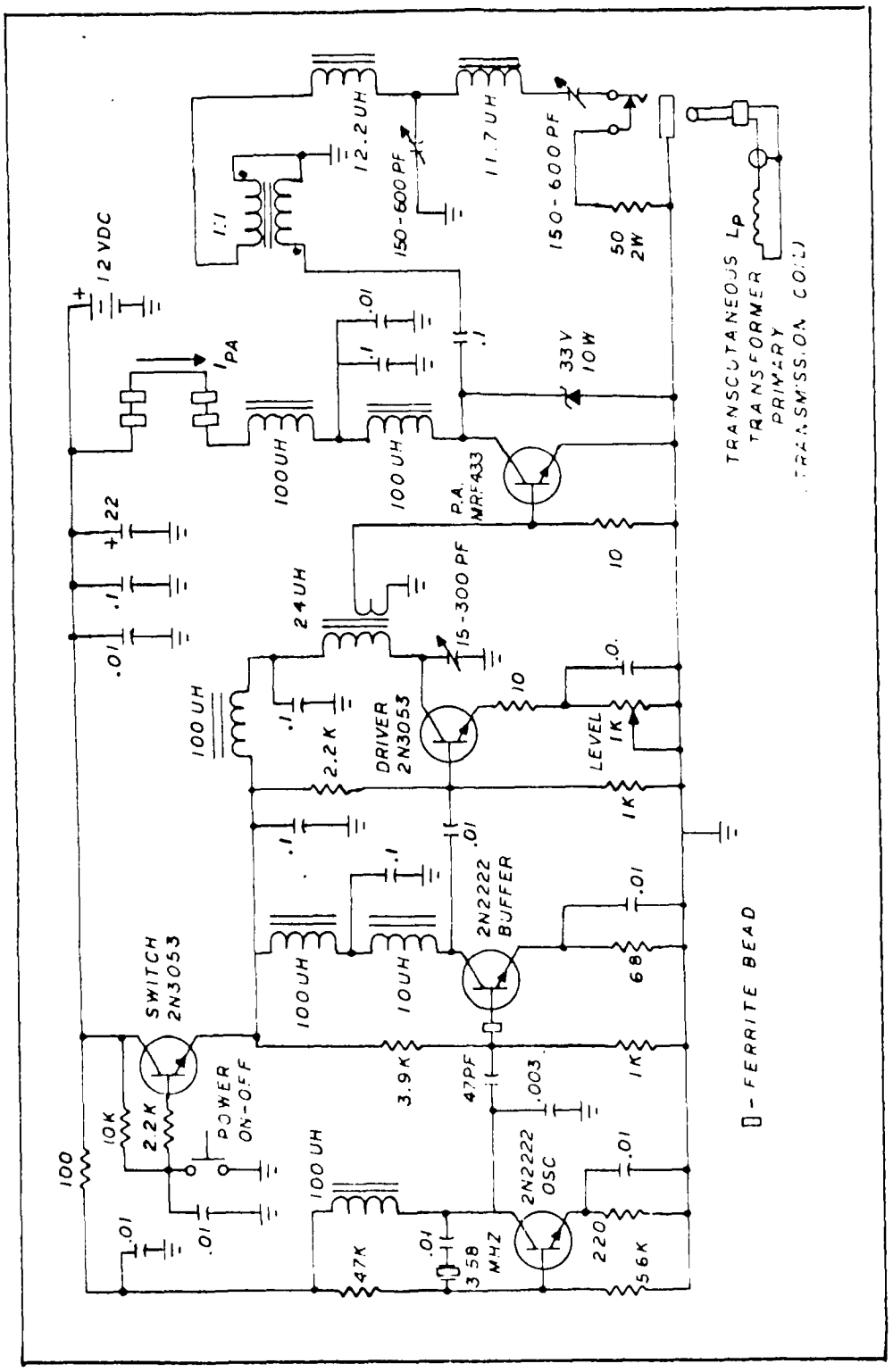


Figure 4.2. External Power Transmitter

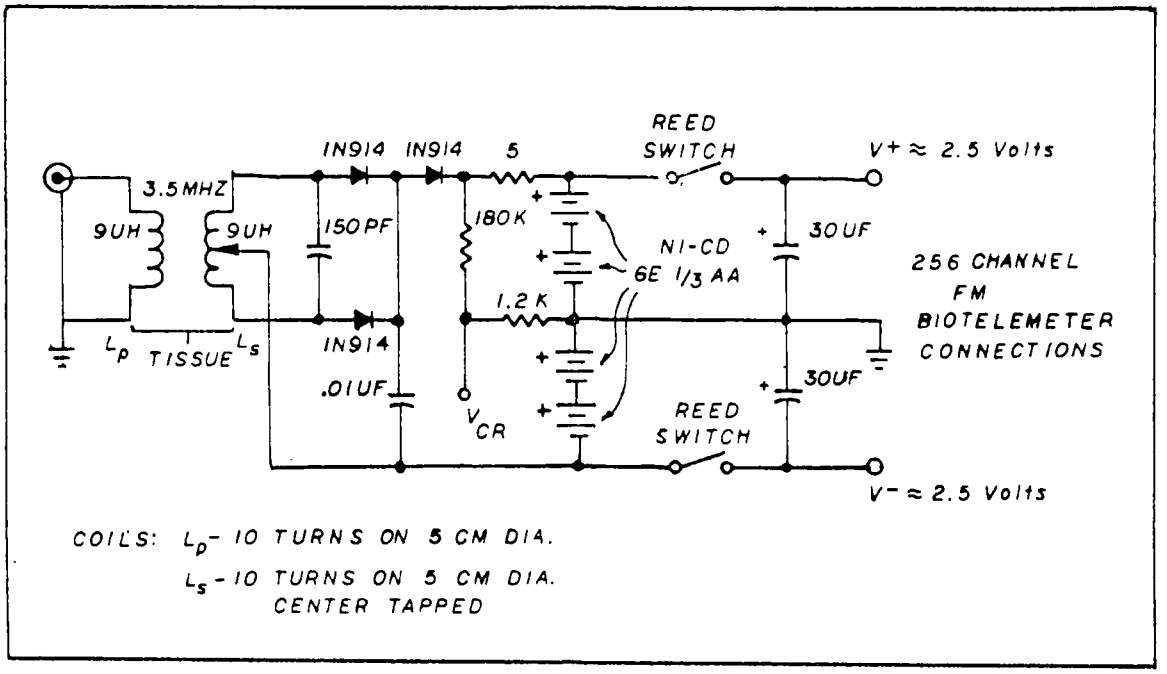


Figure 4.3. Internal Power Supply

The following paragraphs will give a generalized overview of the operation of the system and the modifications required to get the breadboarded version to operate. For more detail than is presented here, the interested reader should read the paper presented by Dr. Jeutter in the IEEE Transactions of Biomedical Engineering, 5 May 1982.

The system used in this application closely follows the block diagram presented in Chapter II for the requirements for the RF powering system. In the front end of the transmitter is a 3.58 MHz crystal controlled Pierce oscillator made using a 2N2222 transistor. This produces a stable sinusoidal oscillation for further power amplification

and filtering. The signal is then power amplified in a 3 stage amplifier section. The 2N2222 buffering stage performs a linear class A amplification of the oscillator output and performs the needed impedance transformation to drive the 2N3053 driver stage. The driver stage performs the first significant level of power amplification. The driver also operates linear class A and has an adjustable gain by varying the amount of DC emitter bias current. The 24 microhenry tuned primary of the coupling transformer between the driver and the power amplifier performs filtering and the 5 turn secondary provides impedance matching to the output amplifier. The power amplifier stage is a high efficiency class C amplifier using a MRF 433 power transistor. The power amplifier drives a tuned T section output stage which provides filtering to a 3.58 MHz sinusoid and impedance transformation from 55 ohms to 50 ohms to allow the use of 50 ohm cabling to connect coupling coils to the unit. The output of the T section is then series tuned with the primary of the transcutaneous coupling transformer to provide maximum power transfer. The supply voltage for the power amplifier is on-off switchable using a 2N3053 transistor as a transistor switch. This allows power conservation when charging is not required and prevents running the unit at a mismatch when positioning the coils. A 33 volt, 10 watt zener diode prevents destruction of the power amplifier transistor when impedance mismatches cause large standing wave ratios in the output section.

The internal section of the powering device is composed of the receiving coil, a full wave rectifier, battery back, and an on-off switch. The receiving coil is a 9 microhenry parallel tuned coil, center tapped to be used as part of a full wave rectifier. A 0.01 microfarad capacitor provides smoothing of the charging voltage from the full wave rectifier. A steering diode and a limiting resistor provide suitable conditions for four series connected General Electric K01X113AA-50-3 Ni-Cd 1.2 volt cells. A low current resistor network allows monitoring of changing voltage to know when the fully charged condition occurs (maximum V_{cr} voltage). This can be used to provide feedback through the biotelemetry link to know when the unit is fully charged, however, this is not implemented in the present design. Magnetic reed switches provide external switchability by the use of close proximity magnets at the skin surface above the reed switch. Two 30 uf capacitors provide supply smoothing and create high frequency current paths through the power supply lines needed for the radio frequency oscillator.

Breadboarding Dr. Jeutter's design required some minor changes in the circuit. The Pierce oscillator as originally configured produced oscillations that went rail to rail causing the 2N2222 buffer stage to be over driven producing a square wave output. To attenuate the oscillation enough to operate the buffer linearly, the 220 pf capacitor from the collector to ground was increased to 3000 pf. Instability in the driver stage at high gains forced a change in the bias

point of the base of 2N3053 driver. Here a 1k ohm resistor was substituted for the 680 ohm resistor to ground. In the receiver unit, the tuning capacitor was changed from 220 pf to 150 pf for better tuning at 3.58 MHz. No other changes of the design were required, however, details of the coils used as transformers were unspecified. After personal conversations with Dr. Jeutter, the coils and transformers were made to the following specifications:

RF Chokes

Size	Type	Core	Turns	Wire Gauge
100 H	High Q	FT 50-67	67	30
100 H	Low Q	FT 50-43	13	22
10 H	Iron core, molded			

Coils and Transformers

Size	Type	Core	Turns	Wire Gauge
12.2 H	High Q	FT 50-67	24	22
11.7 H	High Q	FT 50-67	23	22
24.0 H	High Q	FT 50-67	Primary-33	22
			Secondary-5	22
1:1	High Q	FT 50-67	20	28-Bifilar

Breadboarding was accomplished on a single-sided copper clad perf board with land pattern made by cutting away the copper in narrow strips around the patterns. Areas unused for land pattern formed a suitable ground plane.

Clocking Oscillator

The clocking cscillator provides the necessary clocking signals to sequence through each electrode. To do this, the oscillator must be implant compatible, NMOS electrode array

compatible, low power, and easily reduced to a small package. Within these constraints, the circuit should show good stability over varying power supply voltages and be simplistic for high reliability. The choice of oscillators turned to CMOS designs to provide NMOS compatibility and low power operation. Because the modulator design also requires an inverter to generate an encoded sync pulse, available CMOS inverters were used to design the square wave oscillator (see Figure 4.4) (37:AN88-3).

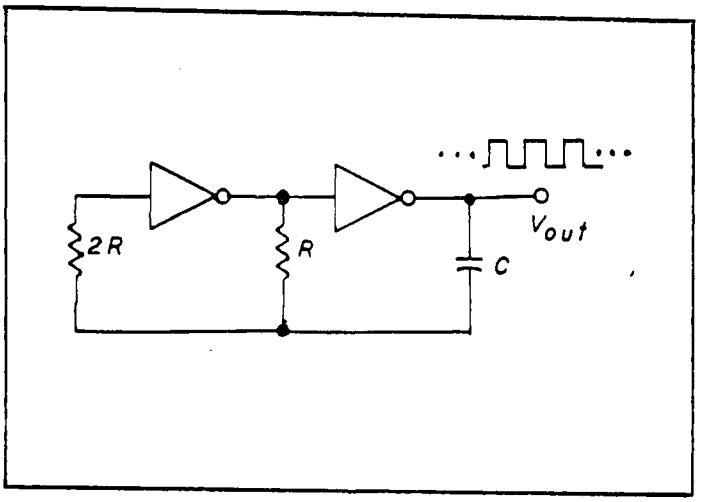


Figure 4.4. Square Wave Oscillator

To make a working oscillator, it is necessary to keep the feedback capacitor fairly small because the output stage of the inverter cannot drive large capacitive loads. Using a 220 pf capacitor and R = 85 kilohms the circuit oscillates at 25 KHz. An adjustable resistor in place of R provides tunability to the desired sampling rate. A complete design

can be seen in Appendix A. In breadboarding the oscillator care must be taken to keep the oscillator far away from the amplifier section and smoothing capacitors must be used on the power supply lines near to the inverter chip. This is needed because the high switching speed of the CMOS devices caused noise spikes on both the power supply lines and in the inputs of the differential instrumentation amplifier, especially as capacitive loading increases. Also to prevent change of oscillation point due to capacitive loading of the output, an inverter should be used as a buffer. If additional power is needed to drive a large capacitive load, several inverters can be used in parallel in the output stage.

V. Circuit Evaluation

Introduction

This chapter describes the testing and evaluation of the breadboarded designs presented in Chapter III and IV. An evaluation will be made whether a system can be built to fulfill the necessary requirements of transmitting through the skin sufficient data to reconstruct the signal of each electrode in the array. Tradeoffs will be discussed as well as their effect on system performance. Finally, system performance with respect to final thick film hybrid will be discussed, pointing out changes needed.

FM Modulator and Demodulator

Test Set Up. To test the operation of the telemetry link, it is necessary, in part, to create a situation similar to the electrode array in the brain environment. Because at the time of this writing an operational version of a fully multiplexed electrode array was not available, the prototype couldn't be tested with a simulated brain signal. To see if the device worked in the range of voltages expected to be seen on the electrode array, an experimental set up was necessary to demonstrate low voltage operation. Available test equipment would only create voltage waveforms at a minimum of 3 to 5 mV so a voltage divider network was necessary to produce accurate working voltages on the order of 20 to 50 microvolts. Source impedance for an electrode can range from 1 kilohm to 20 kilohms, so a 10 kilohm source

impedance R_s was chosen to demonstrate a typical brain electrode. A simple voltage divider using a 10 kilohm resistor as an output and a 620 kilohm resistor as the upper leg reduces the voltage by 63 times, and two 10 kilohm resistors provide the source resistance equivalent to what is produced by an electrode. Figure 5.1 shows the details of the test setup. To monitor the amplified signals an oscilloscope probe was connected to the output of the LM 146 front end amplification stage. Another probe was attached to the output of the baseband amplifier of the phase lock loop demodulator. These test points give a good indication of the sent and received signals making for an easy comparison .

PAM Amplification. Testing of the PAM amplifier seeks to provide a characterization of the signal with respect to noise, distortion, and accurate reproduction of the input PAM staircase signal. First to test the noise in the front amplifier and source resistances, the amplifier was attached to the voltage divider network through 10 kilohm source resistances. With no voltages applied, the network's noise voltage was measured at the output of the PAM amplifier and is snown in Figure 5.2. Since the noise voltage at the input is 950 times less than the displayed value of 4 mV peak to peak, the input noise voltage is approximately 4.5 microvolts. Using a battery applied across the divider network, input noise voltage increased to 7 microvolts before clipping of the output reduced the noise.

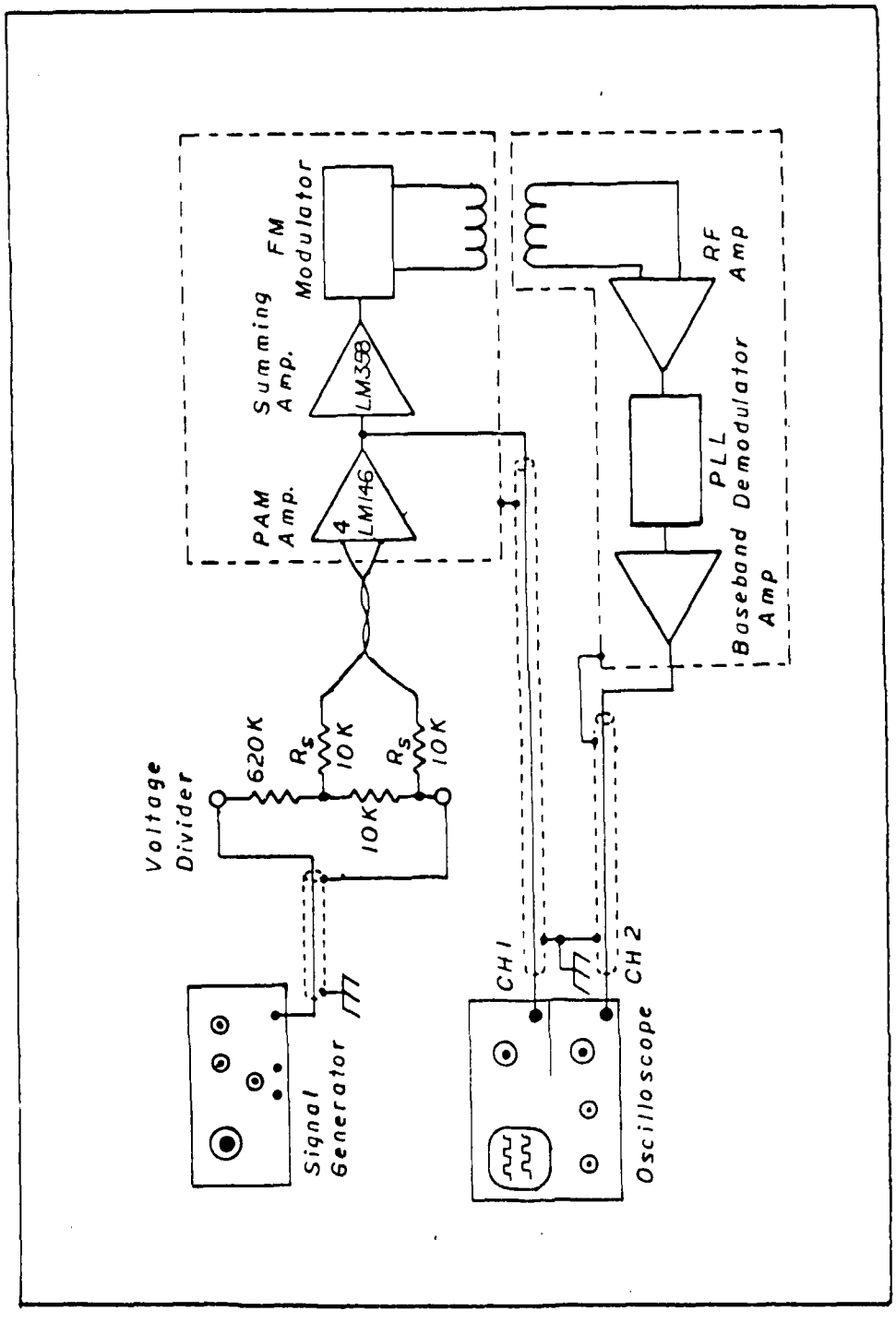
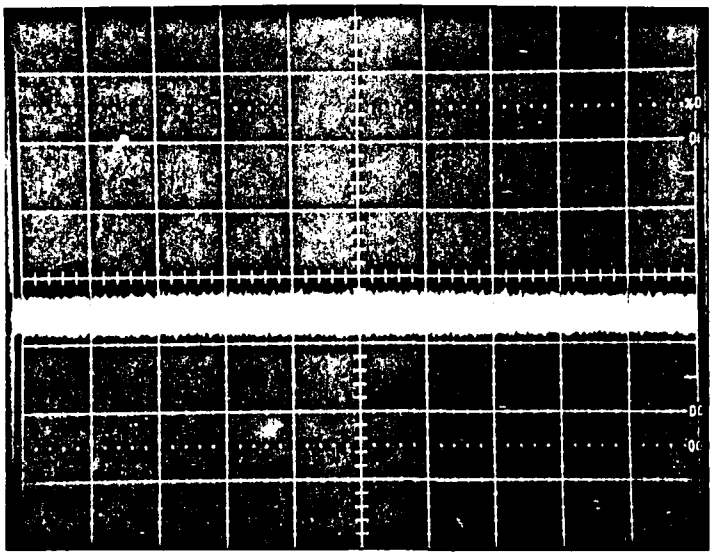


Figure 5.1. Experimental Test Set Up

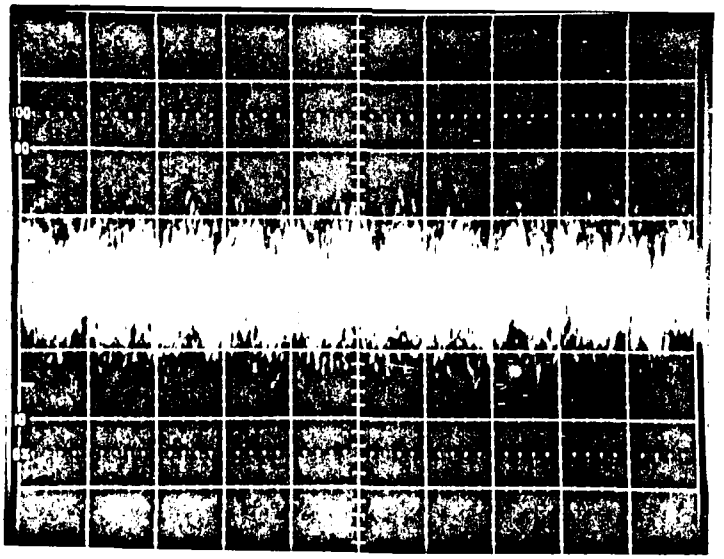


Vert. = 5 mV/div. Horiz. = 50 µs/div.

Figure 5.2. PAM Amplifier Noise with No Input

Clipping of the output occurred because the DC bias produced by the battery, generated a large voltage across the output resistor of the voltage divider which over drives the op amp. Calculating the expected input noise voltage from a input noise voltage of 35 nanovolts per square root of hertz for I_{set} equals 20 microamps, taken from the the table in the data sheets for the LM 146 in Appendix D, and a bandwidth of 150 KHz produces an expected input noise of 13 microvolts. It is expected that the amplifier equivalent noise to be in the range of 10 to 20 microvolts, when an actual signal is applied.

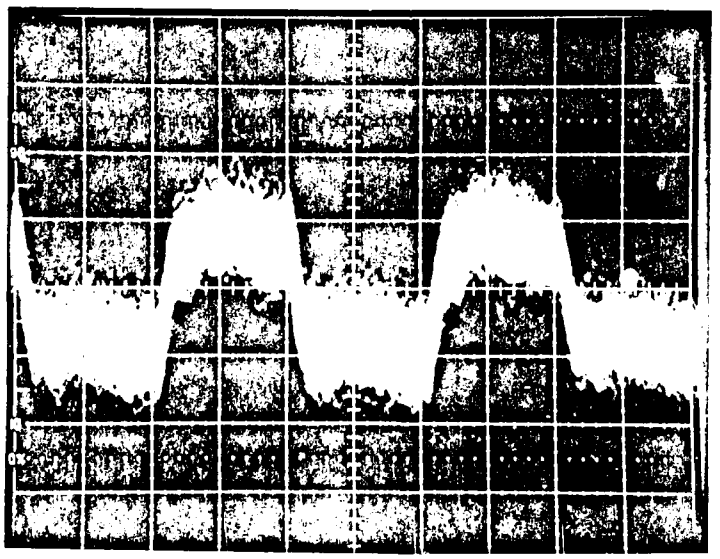
The next step in determining the noise is to apply an actual signal. First the ground lead of a signal generator was attached to the ground of the voltage divider and the output noise recorded (see Figure 5.3). The equivalent average noise voltage at the source is about 46 microvolts. This figure is very high and does not reflect the actual noise in the circuit. External noise from the switching power supply in the signal generator (approximately 22 KHz from Figure 5.3), noise from operating devices in the room, and noise generated in the connecting cables adds to the noise generated by the input amplifiers.



Vert. = 20 mV/div. Horiz. = 50 µs/div.

Figure 5.3. PAM Amplifier Noise with Ground Lead Connection

Using other signal generators gave little improvement, so subsequent measurement and comparison are corrupted by the high amount noise generated in the signal generator and the noise picked up in the connections of the generator to the input. Adjusting the gain of the signal generator for a 45 microvolt square wave, produced the output waveform shown in Figure 5.4. Square wave test inputs of 12.5 KHz were used to demonstrate resolution between the voltages forming the steps in the PAM signal which was multiplexed at 25 KHz. Riding the square wave is 45 microvolts of noise from the generator, and as it shows in the figure, there is a fairly high magnitude sinusoid within that noise likely coming from the generator.

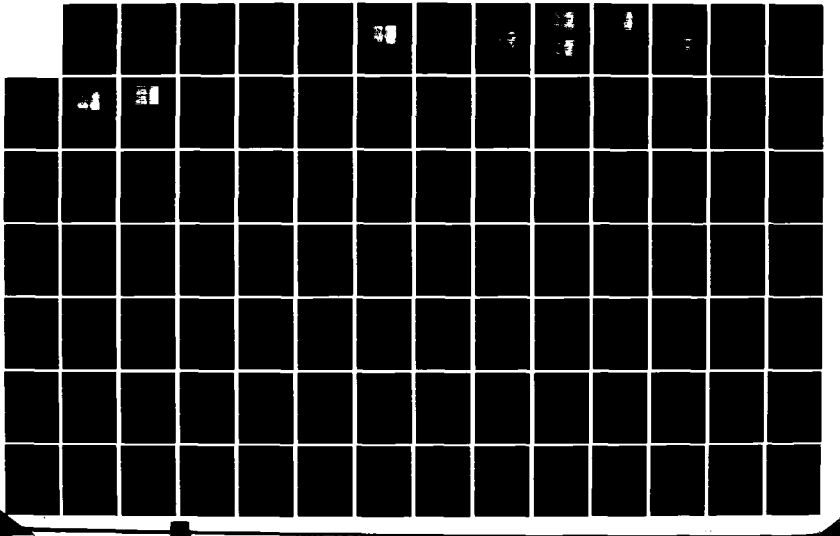


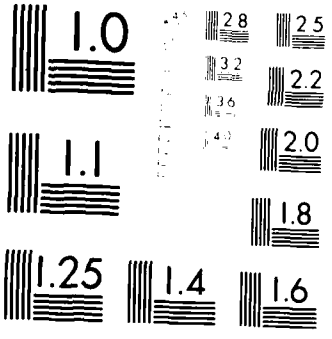
Vert. = 20 mV/div. Horiz. = 20 µs/div.

Figure 5.4. PAM Amplifier Output for a 45 µV Square Wave

AD-A152 238 A COMMUNICATIONS LINK FOR AN IMPLANTABLE ELECTRODE ARRAY(U) AIR FORCE INST OF TECH WRIGHT-PATTERSON AFB OH SCHOOL OF ENGINEERING G S ZEMAN DEC 84 2/3

UNCLASSIFIED AFIT/GE/ENG/84D-70 F/G 6/2 NL





Actual noise in amplification will depend on noise created by the source impedance of the brain, in interfaces between the electrodes and the brain, and the noise in the amplifier itself. From data taken here and calculations made, it's expected that the total noise will be about 10 to 20 microvolts peak to peak allowing a 20 microvolt resolution with good certainty. This will provide adequate resolution for the determination of voltages between electrodes which are commonly between 100 and 200 microvolts.

Rise times and slew rates were also experimentally determined to see if optimum performance could be achieved over various input ranges. At low voltages, rise time due to limited frequency response is the limiting factor on how soon the voltage of the step is stablized and available to be read. A 10% to 90% rise time for a low input voltage signal was measured to be 4 microseconds or one tenth of the electrode period and a 1% to 99% rise time was measured to be 7 microseconds or one fifth of the electrode period. This is consistent with the calculated values given in Chapter II.

Slew rate limitations apply at higher voltages. To determine the slew rates of the amplifier, a 3 mV input signal is applied, forcing the amplifier to switch between saturated states of the op amps. The maximum slew rate is measured by calculating the slope of the rising and falling ramps between states. The results of this calculation are summarized in the following table.

Op Amp Stage	Edge	Slew Rate
LM 146J	Up	650 mV/µs
LM 146J	Down	650 mV/µs
LM 358	Up	260 mV/µs
LM 358	Down(1)	115 mV/µs
LM 358	Down(2)	250 mV/µs

It was noticed that the output stage of the LM 358 which feeds the FM modulator has some very non-linear characteristics. The down sloping slew rate changes about three quarters of the way down. At first a slew rate of 115 mV/us takes place followed by a slew rate of 250 mV/us. The slow slew rate degrades the quality of the transmitted signal by being slower than is needed to produce a stable signal in one fifth of an electrode period . Another characteristic of the LM 358 is overshoot as the voltage approaches one fifth of the supply voltage and causes additional signal degradation as the input signal approaches the 1000 microvolt level. The LM 146J has no slew rate degradation within the operating range of the input signal while the LM 358 degrades at an input level of about 800 microvolts for the down sloping output signal. The choice of LM 358 as the output stage should be reconsidered for subsequent design, especially if output levels to the modulator exceeds 1 volt peak to peak.

Common mode rejection measurement for the unit were taken to see if common potentials on the brain can be

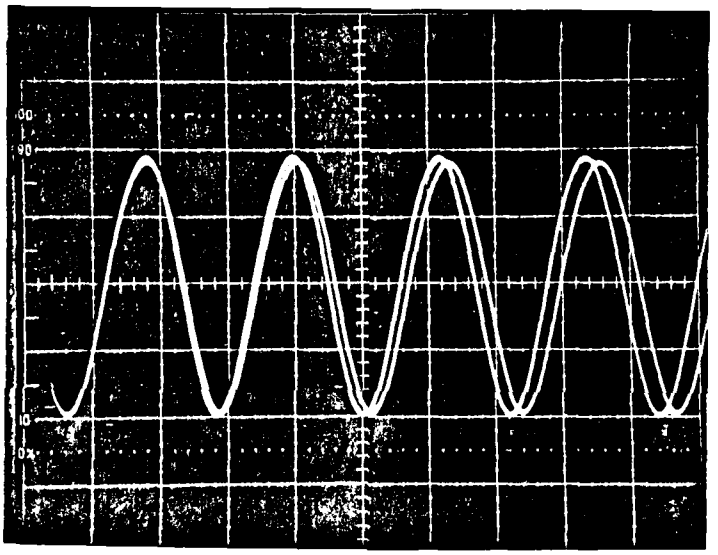
eliminated from the output. The test setup used both a zero source impedance and a 10 kilohm source impedance. In both tests the input signal was taken as a 50 mV peak to peak sinewave, centered around ground, and then each differential input, through their respective source impedances, was connected to the signal generator. For source impedance of zero ohms, the common mode rejection ratio varied from 73 db at 500 Hz to 52 db at 100 kHz and showed slow change until higher frequencies. Using a source impedance of 10 kilohms, the common mode rejection ratio was 67 db at 500 Hz and 50 db at 100 kHz, once again showing slow change until higher frequencies. Due to most of the stray common mode energy being at 60 Hz due to local power lines, common mode rejection for the amplifier is more than sufficient. Improvement in common mode rejection can be made by adhering to stricter tolerances of the resistor values in the differencing amplifier and fine tuning the actual resistor values once the circuit is implemented.

Encoder and Summing Amplifier. The sync encoder and summing amplifier provided adequate synchronization marks to the PAM multiplexed signal. The synchronization mark produced is a negative pulse of about 0.6 volt below the bias voltage at the input of the modulator. The maximum voltage expected due to the electrode is 0.5 volts given a 0.1 volt margin in determining the sync mark. This is more than adequate because noise levels are at 0.02 volts. When the

supply voltage is varied between 5.7 and 4 volts the sync pulse's amplitude shows no appreciable change. The analog switches used to generate the sync pulse generates high speed overshoot transients at the edges of the sync pulse but quickly dampen out. Simulated sync pulse operation shows that an adequate sync can be produced, however it is unknown if the system used to demultiplex can extract the information.

Modulation-Demodulation Testing. Testing of the FM modulator and demodulator was done on a qualitative rather than quantitative basis. Because the signal being input by the voltage divider is corrupted by noise from the signal generator, a visual method of evaluation of the FM modulator/demodulator link is in order. By looking at the collector voltage of the 2N2222A transistor using a 10X probe, the actual output of the transmitting coil can be seen. When the oscillator was allowed to free-run with no signal applied, it oscillated at 8.95 MHz with a variance of + or - 100 Hz. As Figure 5.5 shows, the frequency is modulated by a detectable amount when a 800 microvolt square wave is applied to the input of the PAM amplifier. Also notice that some amplitude modulation does occur as the frequency is shifted, causing some distortion in the transmitted signal. From the picture the difference between the two frequencies is about 200 KHz and in good agreement with predicted values. The input to the FM modulator has

suitable bandwidth since no significant change in the modulation waveforms occur until the 100 KHz cutoff frequency of the PAM amplifier is reached and earlier testing during design stage rated the FM modulator input at about 150 KHz before 3 db attenuation occurred.



Vert. = 1 V/div. Horiz. = 0.05 μs/div.

Figure 5.5 FM Modulation At Collector

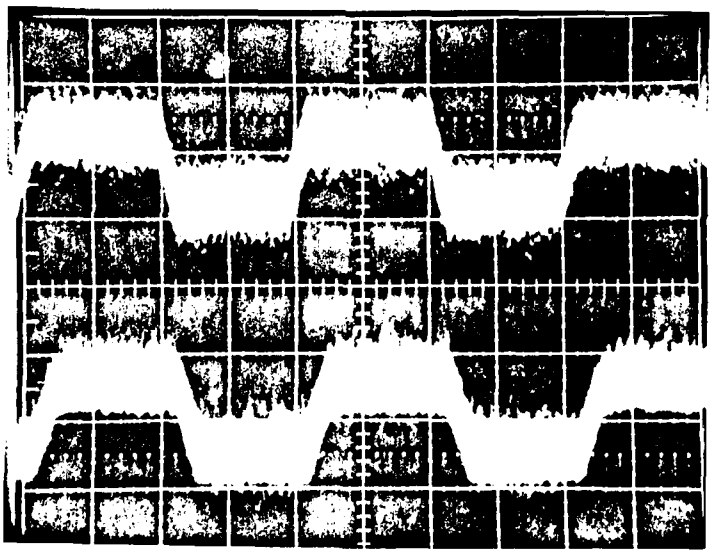
Higher maximum modulation frequencies can be achieved, however reduction of the feedback capacitance, isolation resistor and the Miller capacitance at the collector are needed and makes for a much more difficult design.

Since the transmitting coil will be surrounded by conducting tissue, it was necessary to test the modulator

coil in a saline bath much like the human body would present. A 6% saline solution, much higher than actual body fluid salinity, was used and produced good results. A slight decrease in center frequency was observed as well as a reduction of the peak to peak collector voltage. The resulting detuning of the transmitter coil by the lossy surrounding fluid did not reduce the gain to a point where the oscillator would not run within the input operating range. A slight decrease in oscillator stability was noticed, but changes where gradual and easily tracked out by the PLL as a DC voltage. The design appears to be stable in harsh body environments.

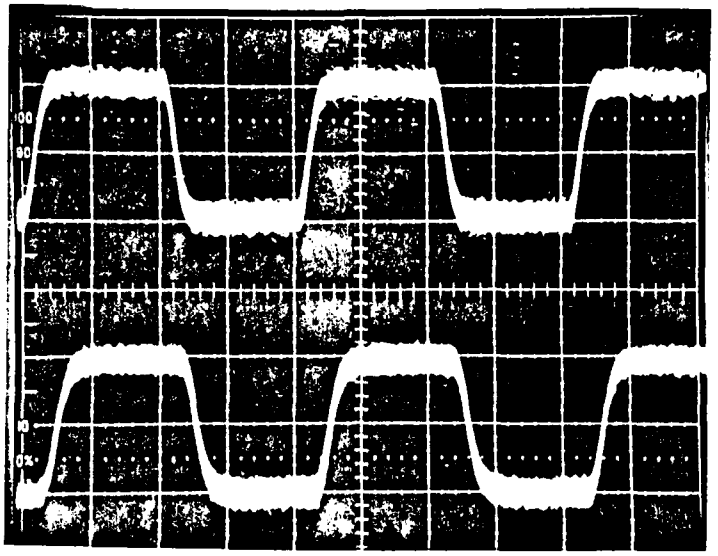
The signal reconstruction capabilities of the FM modulator/demodulator are easily shown by the a direct comparison of input and detected output signals of the system. Antenna coupling for the testing of the link was with a 1 inch coil spacing and a human hand as a surrounding tissue. Once the demodulator system is adjusted as described in Appendix C, the signal at the output of the PAM amplifier and at the output of the demodulated baseband amplifier are compared for accuracy. To more fully see the similarities and differences, the two traces are normalized to the same scale on the screen and shown on the following figures (top is transmitted, bottom is received). The 45 microvolt, 12.5 KHz input signal demonstrates the ability to resolve even the most cluttered signal with a reasonable probability, and a finite difference between electrodes (45 μV) can be detected.

Since the noise is primarily in the signal generator, a more realistic noise is between 2/3 to 1/3 of what is depicted in the photograph. At those levels, 20 microvolts will be resolvable. The 150 microvolt input signal shows the typical step size between adjacent electrodes and is easily resolvable by any post detection system. The 400 microvolt signal shows a typical maximum deviation between adjacent electrodes. Large voltage changes do not cause significant overshoot at these levels.



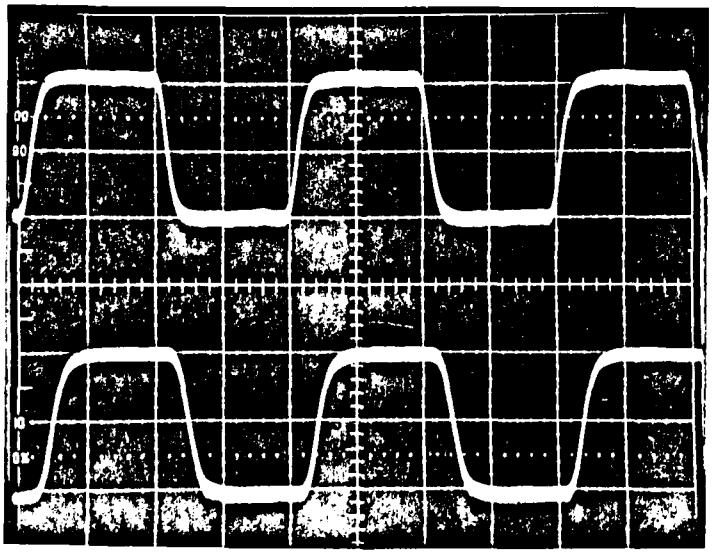
Vert. = uncal. Horiz. = 20 µs/div.

Figure 5.6. Modulation Input and Detected Signal for 45 µV Signal



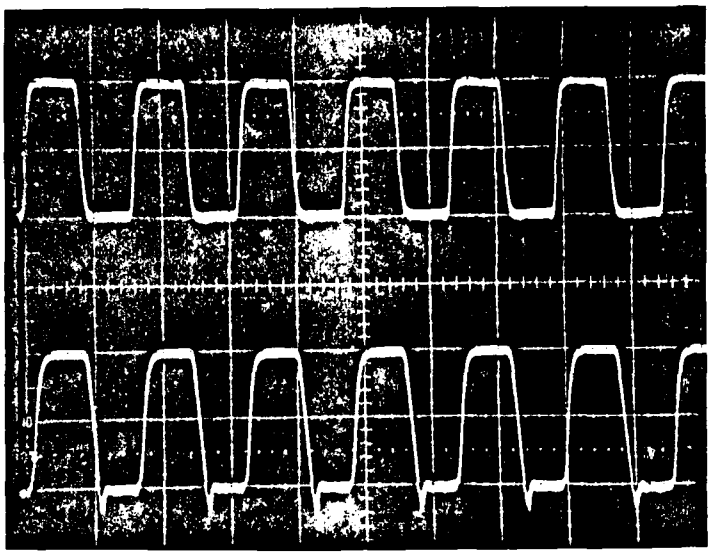
Vert. = uncal. Horiz. = 20 µs/div.

Figure 5.7. Modulation Input and Detected Signal for 150 µV Signal



Vert. = uncal. Horiz. = 20 µs/div.

Figure 5.8. Modulation Input and Detected Signal for 400 µV Signal



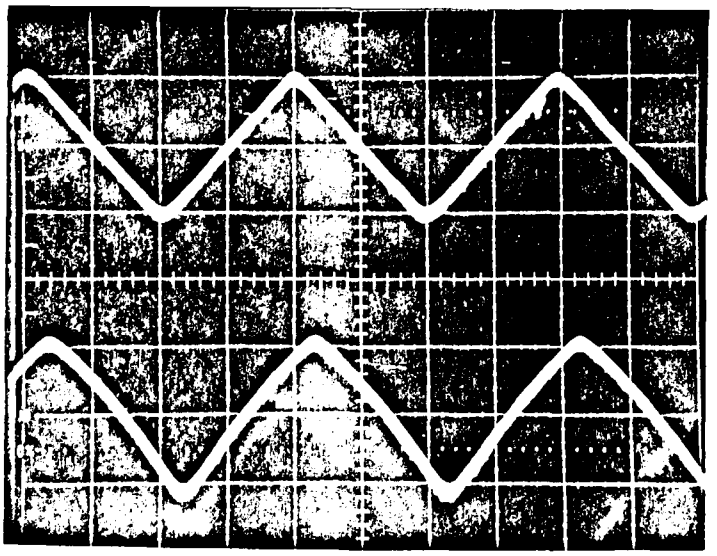
Vert. = uncal. Horiz. = 50 µs/div.

Figure 5.9. Modulation Input and Detected Signal for 1000 µV Signal

The final photograph shows a 1000 microvolt input signal and the non-linear distortion appearing due to the LM 358 op amp. Overshoot is beginning to become significant, and the output is being driven to its maximum slew rate on its downward excursions. This problem should be addressed in a subsequent redesign before a scaled down version is implemented. All of the tests were taken with a 12.5 KHz square wave reflecting a worst case 25 KHz sampling rate. Figures 5.6 through 5.9 show excellent reconstruction of the waveform at the receiver with only minor signal blurring at low input voltage due to the demodulator's voltage controlled oscillator signal bleeding into the ground and output. Higher sampling frequencies can be accommodated, however the

time available for picking off a stablized sample value would be reduced.

The last side by side comparison of the modulator input voltage to an output voltage is given by Figure 5.10. This shows a linear triangle function of 12.5 KHz at 800 microvolts peak to peak and the received shape on the bottom. The distorted waveform received shows the non-linearity of the varactor circuit used to produce frequency modulation. Comparing the shape to the predicted response taken by applying DC bias as in Figure 3.3, shows good agreement. Characteristics of the modulator are exceptable since the transfer function is both predictable and monotonic.



Vert. = uncal. Horiz. = 20 μs/div

Figure 5.10. Modulator Input and Detected Signal for a 800 uV Triangular Signal

The modulator apparatus was then run using various supply voltages to determine the range of the system. Using a variable power supply, the supply voltages were varied and the effect on the circuit monitored. The PAM amplifier was the most dominate in the failure to work at certain supply levels. When the supply voltage reached about 3.8 volts the PAM amplifier discontinued operation. At levels above this point the system operated but quality of the detected signal had degraded. Large input signals had the most noticeable change because of more significant overshoot in the LM 358, loss of frequency response of the op amps, change of modulator bias point, and the reduction of the center frequency. The modulator continued to work through out a 4 to 6 volt range, however loss of percent deviation, reduction of center frequency and the loss of stability occurred at lower voltages. Although the system is not optimum throughout the entire operating range of 4 to 6 volts, the modulator did perform adequately and the demodulator was able to track the changes in the system.

RF Powering Testing

The radio frequency powering circuits was tested for the capacity to operate in various operating conditions, producing reliable and predictable results. Although calibration curves are not presented here, a description of how to generate such a curve once an actual implantation is made will be described. Testing the powering unit involved

checking frequency stabilily, output purity, and the ability to supply desired charging currents. After adjusting the powering unit as specified in Appendix C, the following characteristics were obtained with a 1.5 cm air spacing.

1. Oscillator frequency 3.578950 MHz, + or - 10 Hz

2. Charging current from .1 mA to 150 mA before self oscillation.

3. Power input and charging current peak at distance orginally tuned.

4. 40mA charging current occurs at power supply current at draw of 120 mA.

5. Design is reasonably misalignment tolerant with losses at 15 to 20 % at 1 cm off axis.

6. Output waveform of the transmitter is sinusoidal and of excellent spectral purity.

Characteristics of the RF powering unit show high sensitivity to powering levels used when initial tuning is done. For optimum performance and efficiency, the unit should be tuned at power levels to be used during recharging. Output impedance and loading are highly critical of power levels. High power instability of the driver and output stage (gain potentiometer greater than 3/4) was noticed and attributable to several sources. The beginning of high power instability correspondes to the point where the collector of the power transistor begins being clipped by the 33 volt zener protection diode. This forms a direct current path from the collector of the power transistor and the input of the driver unit through the ground plane and the biasing resistor creating a positive feedback path. Another

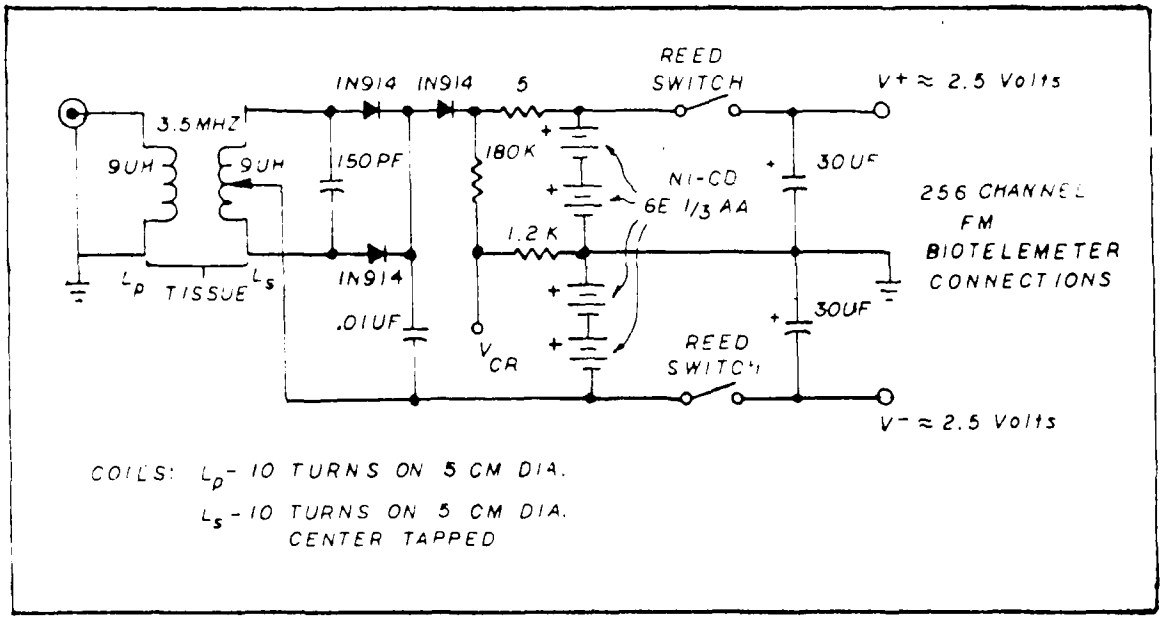


Figure A.4. Internal Power Supply

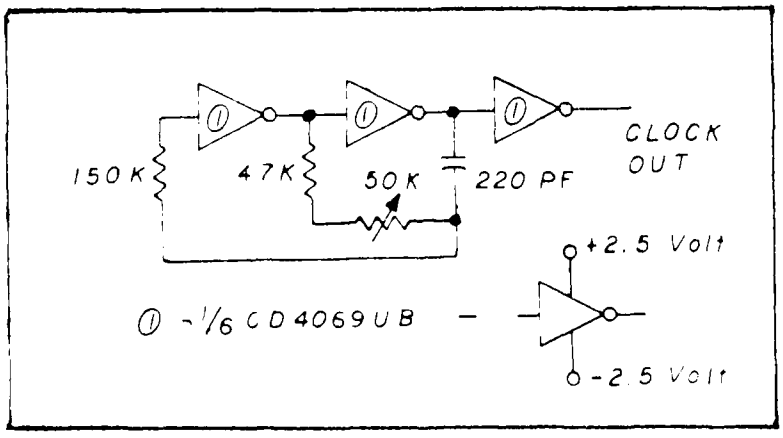


Figure A.5. Clocking Oscillator

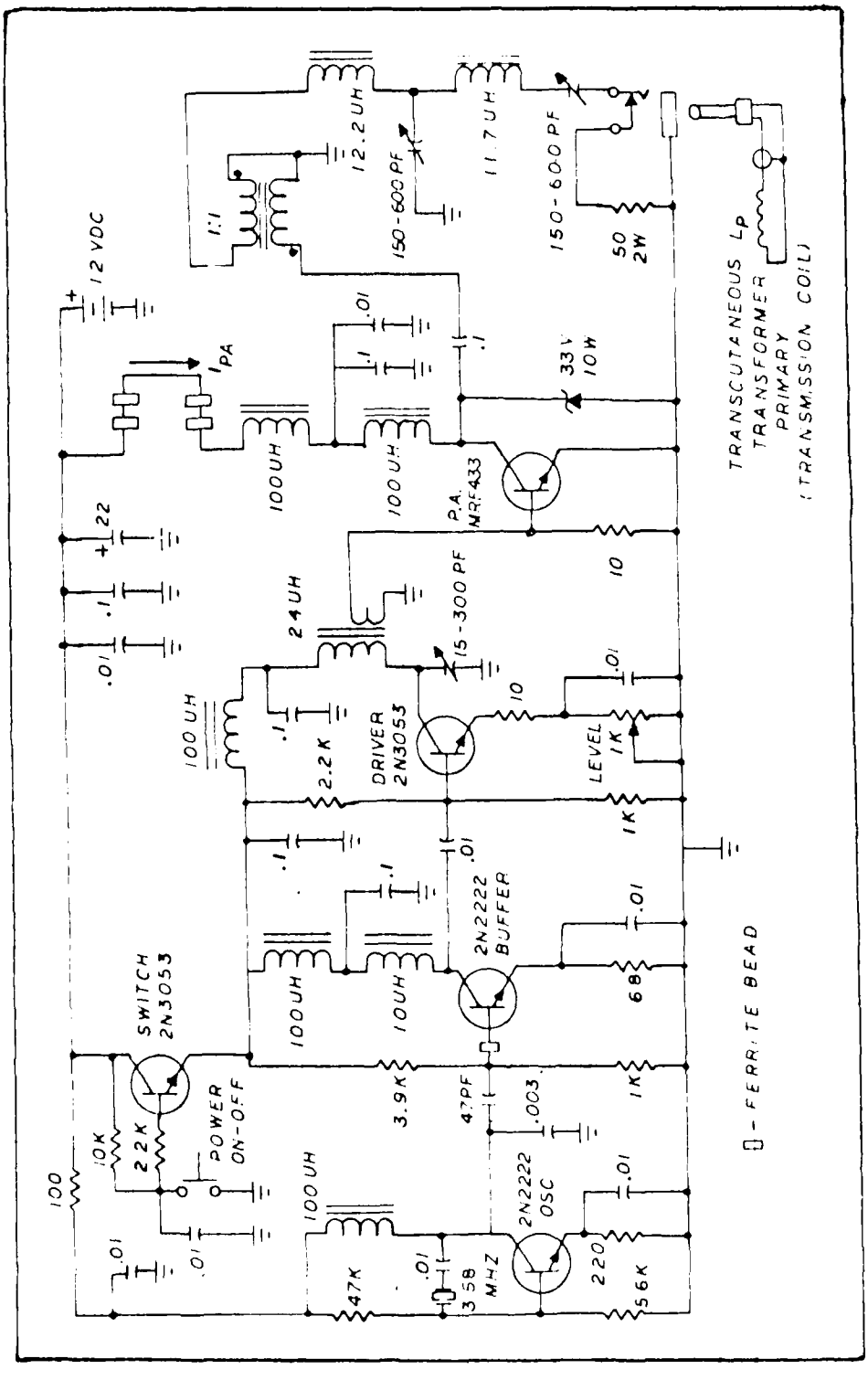


Figure A.3. External RF Powering Transmitter

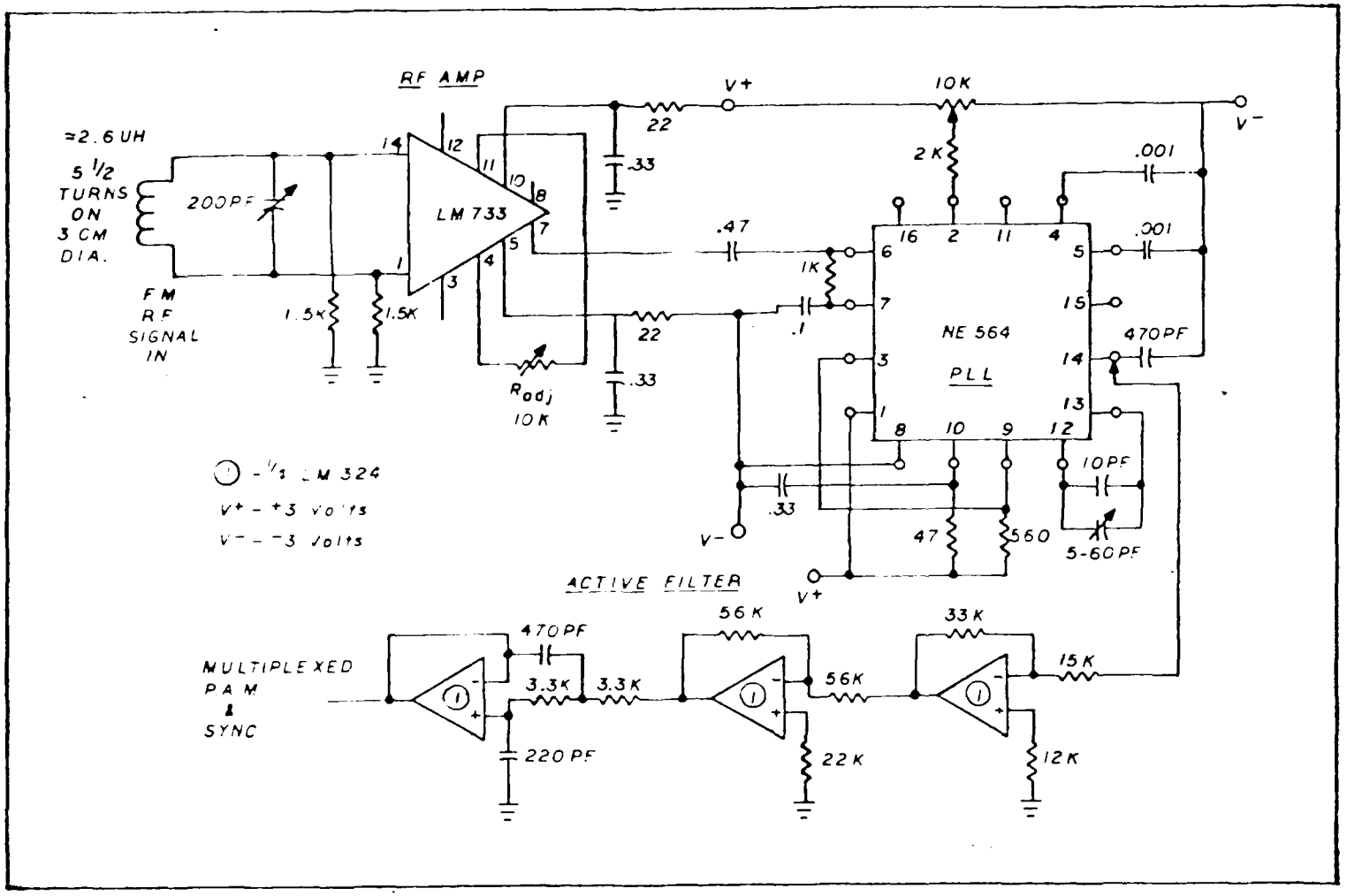


Figure A.2. FM Demodulator

A. Circuit Diagrams

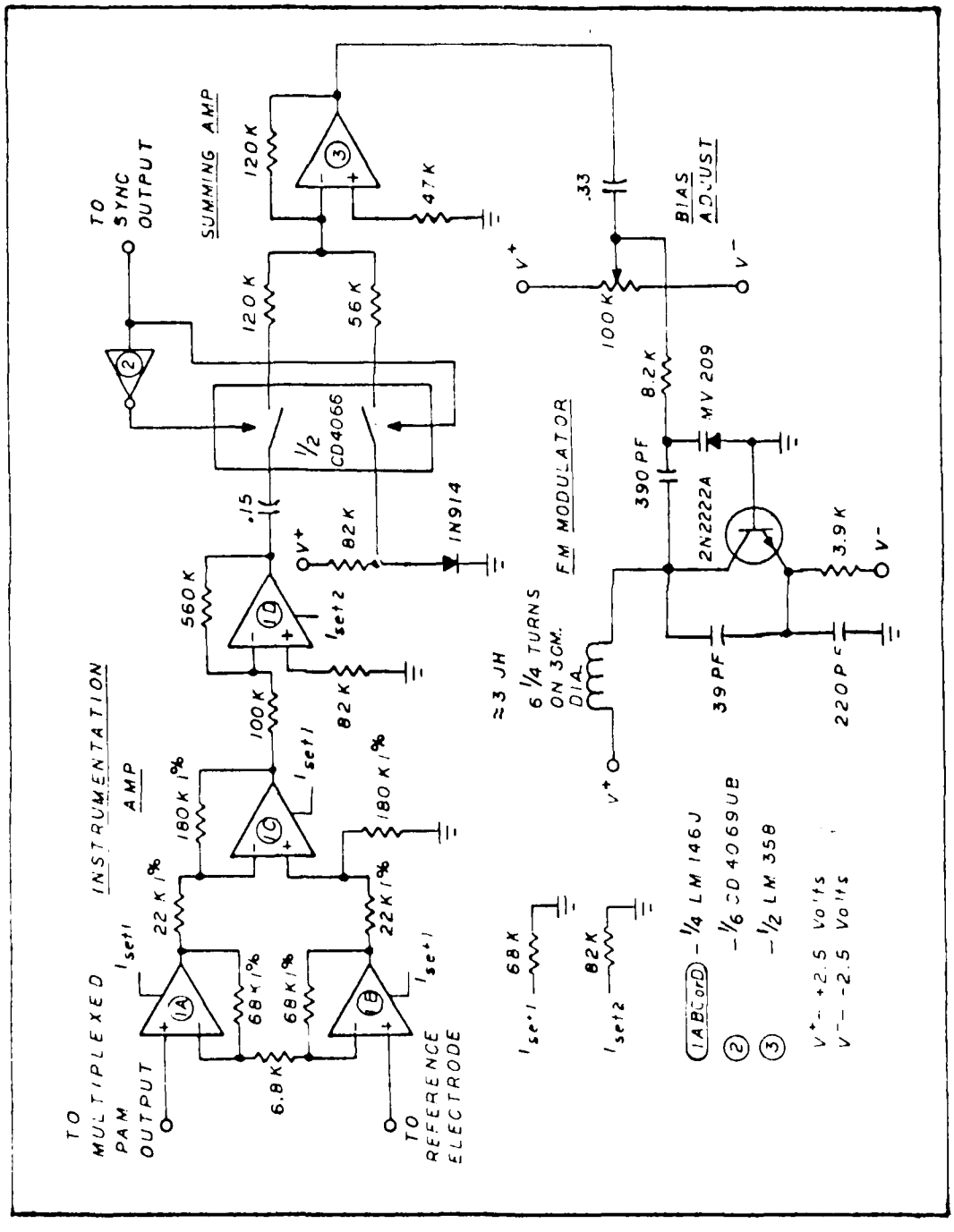


Figure A.1. Amplifier and Modulator

Future Research Areas. The design of this thesis only allows for outward communication of data collected on the brain. To more fully understand the functioning of the brain mapping, a way must be developed to stimulate individual BCE's at will and be able to notice its effects in other areas of the brain. This inward communication system has been proposed, and a feasibility study undertaken by Lin (39:365-366). Parameters which must be controlled externally are: stimulation voltage, frequency of stimulation, pulse width, and whether a particular electrode is on or off. The system could possibly use a small microprocessor to control the sequencing and UART to decode the digital information stream sent by the inward communication link. A simple single electrode stimulator system using an UART and control logic has been developed at Marquette University by Murawski and Jeutter (40:608-611). Such a system would give the capability of a 2 chip total system where data is written to the brain and then the results monitored in another area of the brain. As well as helping to determine a mapping of the visual cortex, the system may allow the generation of visual patterns on the brain for those who have lost their sight due to damage of the visual pathway.

consumption, and since the unit operates at a relatively low frequency of 25 KHz, the dynamic power would be significantly less than the NMOS implementation.

CMOS circuitry also possesses some very useful advantages is design. Current NMOS implementation has limitations of how large of a positive voltage can be passed through a turned on pass transistor without turning it off. This could prove to be a limitation if the array is used as a neural stimulator as described in the next section. CMOS integrated circuits use complimentary gates in parallel for pass transistors which improves on channel resistance and provides a symmetric and full range of allowable input voltages.

The most notable feature of CMOS devices is that a simple CMOS inverter can be used as a high gain amplifier when a bias resistor is placed from output to input (37:AN88-1-3). This design allows them to be treated like an op amp with maximum voltage gains of 40 db and gain-bandwidth products of 10 MHz at the 5 volt supply range. Gains of 10 to 20 at the columns of the array could provide enough gain to get the signal out of the noise on the chip, and then wideband amplification could be used on the fully multiplexed signal without the fear of adding significant noise to the signal. By using this method, much larger arrays could be produced.

than slew rate of the LM 358. Also to be considered in redesign is the FM modulator used for the system. The present system modulates a 9 MHz carrier by 150 KHz or a 2% deviation. For any modulator this is a very large amount of modulation with a non-linear device such as a varactor diode. At a frequency greater than 50 MHz, the deviation of 150 KHz is about 0.4% or less making for a much better linear approximation of the tuning curve. This would also require a redesign of the demodulator to a stable heterodyning front end and a PLL decoder for the frequency translated signal. A high frequency PLL such as Exar XR-520, Signetics NE 560, 561, 562 or individual subsystems made by Motorola and others, allow for better linearity, better signal to noise ratios, and more flexibility in design than the Signetics NE 564 used here. Once these changes to the design are implemented, the design should be laid out as a miniaturized thick film hybrid as described in Appendix F.

Redesign of Electrode Array. It is recommended that the design of the electrode be changed, if possible, to reduce power requirements, improve signal transfer, and provide on board amplification. The present design of the AFIT electrode array is implemented in NMOS with PLA's and pass transistors used to multiplex the signals. The PLA's generates substantial static resistive loading and consumes large amounts of current (20 - 25 mA). The use of CMOS in the design would significantly reduce static power

4. System simplicity allows scalability of breadboarded design to a small hybrid implantable system (Appendix F).

5. Trade-offs of gain, power, bandwidth, and noise within integrated circuit voltage amplifiers limits the multiplexing of unamplified brain signals to level somewhat higher than 256. This makes proposed arrays of thousands of electrodes unfeasible at this time.

6. The probable size of power supply, amplifier and telemetry requires, chest cavity implantation with wires to the electrode array run under the skin.

7. Common mode rejection is sufficient to remove background common mode signals at 5 millivolt levels.

Recommendations

In the progression of this thesis effort, many recommendations came to view which are needed to fully develop a high quality electroencephalogram - telemetry link for large electrode arrays. The areas of recommendation include: redesign for this prototype to a scaled implantable system, redesign of future electrode arrays and future systems using implantable electrode arrays and communications links.

Redesign of FM Telemetry System. To improve the dynamic characteristics of the telemetry link some circuit design changes should be undertaken. First the summing amplifier, modulation driver stage using the LM 358 should be eliminated and the summing amplifier for sync generation incorporated with the last gain stage of the LM 146J. This will reduce power requirements and give the FM modulator a signal limited by frequency response of the amplifier rather

monitoring equipment does not effect the responses, it is possible to increase the understanding of the perception process.

Effective monitoring of a large number of BCE's in the visual cortex requires a long term implantable system where the presence of the system does not evoke unnatural changes in the data collected. Long term implantation will remove the effects of transient localized trauma, infection, anesthetic and antibiotic drugs, and biological rejection. Consistent and accurate data collected in this way, are required to develop a good model of the actual transformation occurring between the primary and secondary visual cortex.

The system developed by this thesis shows that it is feasible to build a system using commonly available integrated circuits which can transcutaneously couple out the data produced from a 256 electrode array. From the results of the bread boarded prototype of the system, the following conclusions are drawn:

1. High bandwidth (100 KHz) and low power (18 milli-watt) implantable electroencephalographic communication channels can be made but at the expense of increased noise (10 - 20 microvolts) and associated loss of signal voltage resolvability.

2. Signal to noise limitations of telemetry system are due to the front end (PAM) amplification of low level brain signals rather than by the FM communications link.

3. Single frequency RF powering of rechargable cells provides a suitable power source for high current (35 mA), short usage (less than 2 hours) systems, and adds the capability for long term implantability.

VI. Conclusions and Recommendations

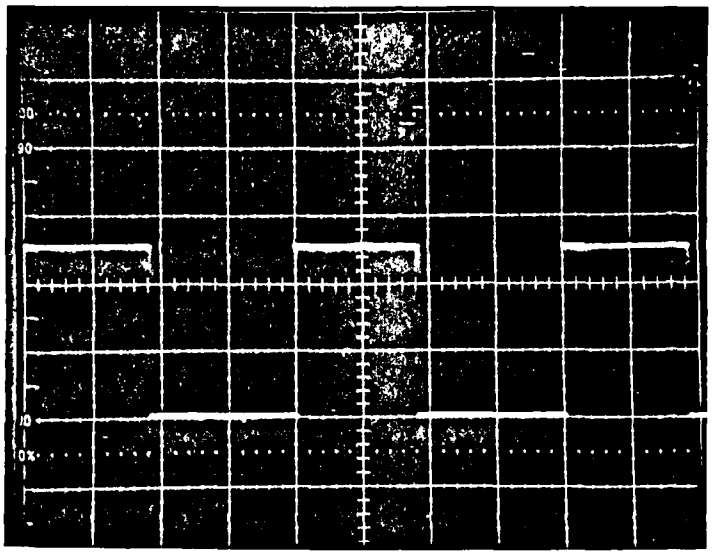
Introduction

An investigation into the past research and the underlying theory involved in the visual information processing system was conducted. That investigation produced the need for an implantable system which can transcutaneously transmit data from the implanted electrode array and receive external power from a signal frequency source. To test the feasibility of such a system, a design was developed and tested. This chapter contains the conclusion and recommendations resulting from the investigation of a system suitable to transmit the electrode array data transcutaneously.

Conclusions

Testability of the hypothesis of Fourier type transformation by the mammalian visual system for pattern recognition requires the monitoring of large number of BCE's in the visual pathway. Evidence has shown that due to the lack of lateral information transfer in the primary visual cortex, spatial pattern recognition does not occur there. A complex interconnection of points in the primary visual cortex to many points in the secondary or association area imply that the first level of visual information processing occurs here. By exploring the nature of the interconnection between primary and association areas,in an environment where

fidelity to reproduce the PAM and Sync information outside the brain cavity without any breaks in the skin. From the breadboarded prototype, definite conclusions on the ability to form a reliable long term telemetry link can be drawn. Scalability, a key to the realization of an implantable system is covered in Appendix F.



Vert. = 2 v/div. Horiz. = 10 µs/div.

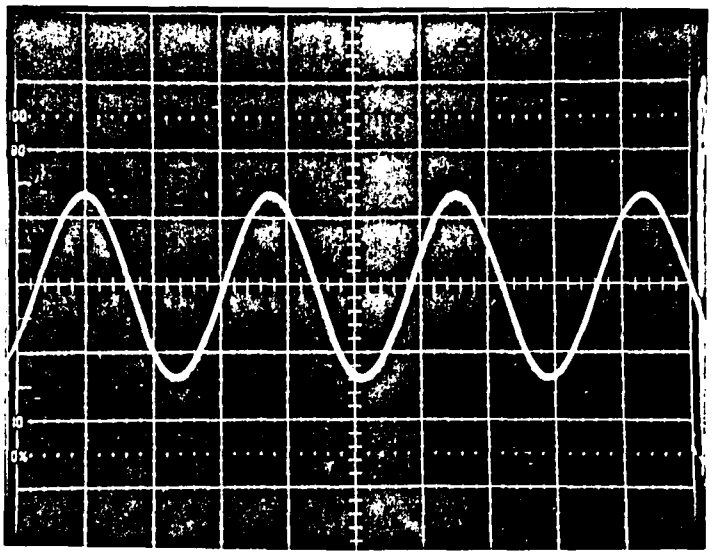
Figure 5.12. Electrode Array Clocking Oscillator

Variations of frequency over applied voltage range of 5.7 to 4 volts were + or - 600 hertz.

The fast rise times of the inverters cause some problems with power supply noise and coupling noise from the oscillator to amplifier input lines. Large capacitive loads further degrade the system with switching noise. Fairly large storage (smoothing) capacitors should be used near the oscillator and the oscillator, should be placed so short lines connect it to the electrode array. If additional driving current is needed, the output buffer inverter can be ganged in parallel to produce sufficient drive currents.

The design proven in this thesis shows that a low power transmitter and rechargable unit can be made with sufficient

demodulator's ground. Battery pack performance should be suitable for routine data taking over a several year period.



Vert. = 50 V/div. Horiz = 0.1 μs/div.

Figure 5.11 RF Transmitter Coil Voltage

Clocking Oscillator Testing

The clocking oscillator testing involved the adjustability of oscillator frequency and the ability to produce a stable accurate clock compatible with NMOS circuitry. The oscillator is easily tuned by adjusting the variable 50 kilohm resistor depicted in Figure A.5 in appendix A, producing a range from 18 KHz to 27 Khz with extended ranges possible. Once set at 25 KHz, the oscillator varied no more than 100 Hz and provided excellent crisp edges, see Figure 5.12.

possible source of self oscillation is the coupling due to leakage currents bleeding off the square edged land patterns defining circuit paths. At a 40 mA charging current, measured at the Ni-Cd cells, the voltage measured at the series tuning capacitor of the output stage shows a peak to peak voltage of 140 volts (see Figure 5.11). The waveform is an excellent sinusoid with very little distortion. At 40 mA, batteries are charged to full charge in 3 hours and stabilize at 5.7 volts. For additional characteristics of the power supply see Dr. Jeutter's paper (36:314-321).

Testing the battery pack involved running the system at an equivalent load. First the system was run using the PAM amplifier and FM modulator. The unit was started by magnet switching of the reed switches through tissue simulated by a human hand and the unit immediately began to transmit. Current drawn for the amplifier and the FM modulator was 3.2 milliamps in both the positive and negative supplies with an insignificant current flow through ground. Then the batteries were recharged and a 250 ohm resistor was used to represent the 20 mA draw of the electrode array. The unit was run for 2 hours with no significant degradation of performance. A peculiarity in the system was noticed when running, in that the grounds of the two systems (modulator and demodulator) must be coupled to prevent the detection and output of large impulsive switch spikes from near by equipment. Coupling needed only be weak (highly resistive) and can be accomplished through a common ground using tissue for the implant's ground and a skin electrode as the

B. Equipment List

1. Hewlet Packard, Clip On DC Milliameter Model 4288
2. Hewlet Packard, Electronic Counter Model 5246L
3. Hewlet Packard, Triple Output Power Supply O-6V-2.5A/0 +or- 20V-.5A Model 6236B
4. John Fluke Manufacturing, Digital Multimeter Model 8100B
5. Tektronics, Oscilloscope Model AN/USM-425(V)-1
6. Wave-Tek, 20 MHz AM/FM/PM Generator Model 148

C. Adjustment Procedures

FM Demodulator Adjustment

1. Before applying power remove PLL NE-564 from its socket, then connect power supply and power up the demodulator board

2. Turn on the FM modulator unit and place the receiver loop in position alignned with transmitter coil. Using an oscilloscope, monitor the output, pin 7, of the video amplifier, LM 733, while tuning the variable capacitor in parallel with the receiving coil. Adjust for maximum peak to peak voltage. Then adjust gain resistor for output level of 150 mV.

3. Turn off FM modulator unit, and demodulator unit. Replace PLL chip NE 564 in socket. Turn on power to demodulator only.

4. Using a frequency counter, monitor the frequency of the voltage controlled oscillator at pin 3 of the PLL chip. Adjust variable frequency set capacitor for an 8.5 MHz reading. This should be slightly lower than expected frequency of modulator due to loading of oscillator by the probe, but exact frequency is not critical. Remove frequency monitoring equipment.

5. Turn on FM modulator unit. Using an oscilloscope, watch the signal output at the end of the baseband filtering stage. Slowly adjust the frequency set capacitor of the phase lock loop until a signal locks at the output. Slowly adjust through the lock condition noticing the signal quality

through out the locked range. Set the tuning capacitor to the best lock condition. This may not be sufficient to hold lock over entire waveform.

6. To achieve a more complete lock and the cleanest waveform, the bias current at pin 2 must be adjusted. While watching the output of the baseband amplifier slowly vary the potentiometer until complete lock occurs. Because the bias current changes center frequency, step 5 should be repeated as the bias current is adjusted. Once complete locking occurs, continue adjusting until the stepped response has clean edges and overshoot has been minimized. Care should be taken to repeat step 5 throughout the procedure to insure good center frequency positioning.

7. The next step is to readjust the front end receiver. The variable capacitor in parallel to the receiving coil should be slowly tuned to produce the cleanest waveform. Small changes can produce large changes so care must be exerised in changing frequency. Mildly retune as in steps 5 and 6 to produce optimum system configuration.

RF Powering Adjustments

1. Making sure that powering section is off and the plug-in powering coil is disconnected, connect the power supply to the unit.

2. Adjust the driver's tank tuning capacitor for a mid-adjustment. Adjust each of the two 600 pf variable capacitors to three quarters of full capacitance position.

Finally adjust the variable one kilohm gain potentiometer so it is two thirds to three quarters of full value.

3. Connect a 10X probe from an oscilloscope to the 50 ohm output resistor. Also place a DC current meter clamp on the loop in the collector of the power amplifier.

4. Turn on the power amplifier stage and monitor the current and voltage at each of the points desribed above. Slowly adjust the driver tuning capacitor until max current at the collector and maximum output voltage at the 50 ohm resistance is seen.

5. Adjust tuning capacitor in the T section impendance transformation network until max current at the collector and max voltage at the 50 ohm resistor are seen. Repeat step 4, then this step again.

6. Turn off power to power amplifier and attach the power transmission coil to the unit. Place the coil in the proper orientation for operation with implanted unit. Remove oscilloscope probe from 50 ohm resistor and place on insultated cable of the transmission coil. Power level in the cable are significant enough to be capacitively coupled to the scope probe and can be used as a good indication of power level without loading circuit.

7. Turn on power to the power amplifier. While monitoring both current at the collector and voltage in the transmission coil adjust the series tuning capacitor in the output stage for max current and voltage. Once again repeat steps 4 and 5 while monitoring the voltage in the transmission coil and

then readjust the series tuning capacitor. Repeat until no further gains can be achieved.

8. Compare current draw to expected value determined by tests made on the circuit before implantation for a particular battery charging current. If a change is desired, adjust the one kilohm gain control until appropriate current is seen and readjust tuning capacitors as in Steps 4, 5, and 7 until optimum performance is achieved.

9. If coil is used constantly in the same orientation, no further adjustments are needed for future charging of the batteries.

D. Data Sheets

This appendix presents the data sheets of the devices used in the design of the prototype communications link. The purpose of their placement in this thesis is for a quick reference of the properties of the devices chosen. The data sheets also supply necessary design equations and information used to develop the link. This information will provide the ability to specify other integrated circuits and active devices to take the place of the ones used if the devices are unavailable.

National Semiconductor

Operational Amplifiers/Buffers

LM158/LM258/LM358, LM158A/LM258A/LM358A, LM2904 Low Power Dual Operational Amplifiers

General Description

The LM158 series consists of two independent, high gain, internally frequency compensated operational amplifiers which were designed specifically to operate from a single power supply over a wide range of voltages. Operation from split power supplies is also possible and the low power supply current drain is independent of the magnitude of the power supply voltage.

Application areas include transducer amplifiers, dc gain blocks and all the conventional op amp circuits which now can be more easily implemented in single power supply systems. For example, the LM158 series can be directly operated off of the standard +5 V_{DC} power supply voltage which is used in digital systems and will easily provide the required interface electronics without requiring the additional ±15 V_{DC} power supplies.

Unique Characteristics

- In the linear mode the input common-mode voltage range includes ground and the output voltage can also swing to ground, even though operated from only a single power supply voltage.
- The unity gain cross frequency is temperature compensated.
- The input bias current is also temperature compensated.

Advantages

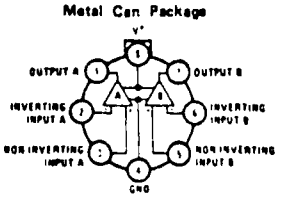
- Eliminates need for dual supplies
- Two internally compensated op amps in a single package
- Allows directly sensing near GND and V_{OUT} also goes to GND
- Compatible with all forms of logic
- Power drain suitable for battery operation
- Pin-out same as LM1558/LM1458 dual operational amplifier

Features

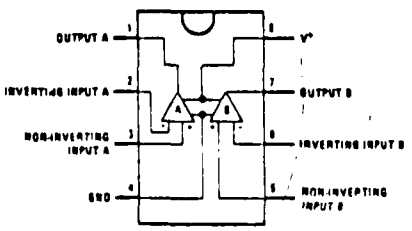
- Internally frequency compensated for unity gain
- Large dc voltage gain — 100 dB
- Wide bandwidth (unity gain) (temperature compensated) — 1 MHz
- Wide power supply range
  - Single supply — 3 V_{DC} to 30 V_{DC}
  - or dual supplies — ±1.5 V_{DC} to ±15 V_{DC}
- Very low supply current drain (500μA) — essentially independent of supply voltage (1 mW/op amp at +5 V_{DC})
- Low input biasing current (temperature compensated) — 45 nA_{DC}
- Low input offset voltage — 2 mV_{DC}
- and offset current — 5 nA_{DC}
- Input common-mode voltage range includes ground
- Differential input voltage range equal to the power supply voltage
- Large output voltage swing — 0 V_{DC} to V^+ − 1.5 V_{DC}

Connection Diagrams (Top Views)

Metal Can Package

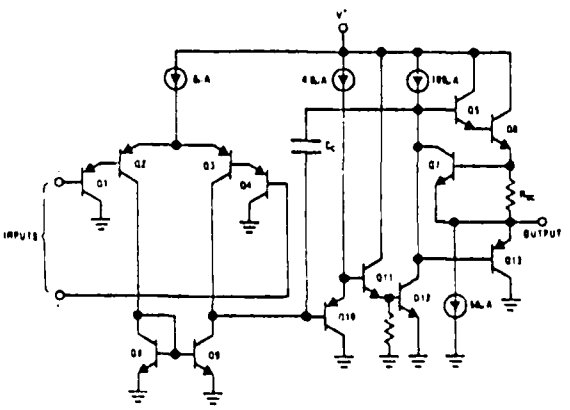


Order Number LM158AH, LM158H, LM258AH, LM258H, LM358AH or LM358H
See NS Package H08C



Order Number LM358AN, LM358N or LM2904N
See NS Package N08B

Schematic Diagram (Each Amplifier)



Absolute Maximum Ratings

	LM158/LM258/LM358 LM158A/LM258A/LM358A	LM2904
Supply Voltage, V^+	32 V_{DC} or ±16 V_{DC}	26 V_{DC} or ±13 V_{DC}
Differential Input Voltage	32 V_{DC}	26 V_{DC}
Input Voltage	−0.3 V_{DC} to +32 V_{DC}	−0.3 V_{DC} to +26 V_{DC}
Power Dissipation (Note 1)		
Molded DIP (LM358N)	570 mW	570 mW
Metal Can (LM158H/LM258H, LM358H)	830 mW	
Output Short Circuit to GND (One Amplifier) (Note 2) $V^+ \leq 15$ V_{DC} and $T_A = 25°C$	Continuous	Continuous
Input Current ($V_{IN} < -0.3$ V_{DC}) (Note 3)	50 mA	50 mA
Operating Temperature Range		
LM358	0°C to +70°C	−40°C to +85°C
LM258	−25°C to +85°C	
LM158	−55°C to +125°C	
Storage Temperature Range	−65°C to +150°C	−65°C to +150°C
Lead Temperature (Soldering, 10 seconds)	300°C	300°C

Electrical Characteristics ($V^+ = +5.0$ V_{DC}, Note 4)

PARAMETER	CONDITIONS	LM158A			LM258A			LM358A			LM158/LM258			LM358			LM2904			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
Input Offset Voltage	$T_A = 25°C$, (Note 5)		1	2		1	3		2	3		±2	±5		±2	±7		±2	±7	mV_{DC}
Input Bias Current	$I_{IN(+)}$ or $I_{IN(-)}$, $T_A = 25°C$, (Note 6)		20	50		40	80		45	100		45	150		45	250		45	250	nA_{DC}
Input Offset Current	$I_{IN(+)} - I_{IN(-)}$, $T_A = 25°C$		2	10		2	15		5	30		±3	±30		±5	±50		±5	±50	nA_{DC}
Input Common Mode Voltage Range	$V^+ = 30$ V_{DC}, $T_A = 25°C$ (Note 7)	0		$V^+-1.5$	0		$V^+-1.5$	0		$V^+-1.5$	0		$V^+-1.5$	0		$V^+-1.5$	0		$V^+-1.5$	V_{DC}
Supply Current	$R_L = \infty$, $V_{CC} = 30V$ (LM2904 $V_{CC} = 26V$)		1	2		1	2		1	2		1	2		1	2		1	2	mA_{DC}
	$R_L = \infty$ On All Op Amps		0.7	1.2		0.7	1.2		0.7	1.2		0.7	1.2		0.7	1.2		0.7	1.2	mA_{DC}
	Over Full Temperature Range																			
Large Signal Voltage Gain	$V^+ = 15$ V_{DC} (For Large V_O Swing) $R_L \geq 2$ kΩ, $T_A = 25°C$	50	100		50	100		25	100		50	100		25	100			100		V/mV
Output Voltage Swing	$R_L = 2$ kΩ, $T_A = 25°C$ (LM2904 $R_L \geq 10$ kΩ)	0		$V^+-1.5$	0		$V^+-1.5$	0		$V^+-1.5$	0		$V^+-1.5$	0		$V^+-1.5$	0		$V^+-1.5$	V_{DC}
Common Mode Rejection Ratio	DC, $T_A = 25°C$	70	85		70	85		65	85		70	85		65	70		50	70		dB
Power Supply Rejection Ratio	DC, $T_A = 25°C$	65	100		65	100		65	100		65	100		65	100		50	100		dB
Amplifier to Amplifier Coupling	f = 1 kHz to 20 kHz, $T_A = 25°C$ (Input Referred), (Note 8)		−120			−120			−120			−120			−120			−120		dB
Output Current Source	$V_{IN}^+ = 1$ V_{DC}, $V_{IN}^- = 0$ V_{DC}, $V^+ = 15$ V_{DC}, $T_A = 25°C$	20	40		20	40		20	40		20	40		20	40		20	40		mA_{DC}

Electrical Characteristics (Continued) (V^+ = +5.0 V_{DC}, Note 4)

PARAMETER	CONDITIONS	LM158A			LM258A			LM358A			LM158/LM258			LM358			LM2904			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
Sink	V_{IN}^- = 1 V_{DC}, V_{IN}^+ = 0 V_{DC}, V^+ = 15 V_{DC}, T_A = 25°C	10	20		10	20		10	20		10	20		10	20		10	20		mA_{DC}
	V_{IN}^- = 1 V_{DC}, V_{IN}^+ = 0 V_{DC}, T_A = 25°C, V_O = 200 mV_{DC}	12	50		12	50		12	50		12	50		12	50					μA_{DC}
Short Circuit to Ground	T_A = 25°C (Note 2)		40	60		40	60		40	60		40	60		40	60		40	60	mA_{DC}
Input Offset Voltage	(Note 5)			4			4			5			±7			±9			±10	mV_{DC}
Input Offset Voltage Drift	R_S = 0Ω		7	15		7	15		7	20		7			7			7		$\mu V/°C$
Input Offset Current	$I_{IN(+)} - I_{IN(-)}$			30			30			75			±100			±150		45	±200	nA_{DC}
Input Offset Current Drift			10	200		10	200		10	300		10			10			10		$pA_{DC}/°C$
Input Bias Current	$I_{IN(+)}$ or $I_{IN(-)}$		40	100		40	100		40	200		40	300		40	500		40	500	nA_{DC}
Input Common-Mode Voltage Range	V^+ = 30 V_{DC} (Note 7)	0		$V^+ - 2$	0		$V^+ - 2$	0		$V^+ - 2$	0		$V^+ - 2$	0		$V^+ - 2$	0		$V^+ - 2$	V_{DC}
Large Signal Voltage Gain	V^+ = +15 V_{DC} (For Large V_O Swing), $R_L \geq 2$ kΩ	25			25			15			25			15			15			V/mV
Output Voltage Swing																				
V_{OH}	V^+ = +30 V_{DC}, R_L = 2 kΩ	26			26			26			26			26			22			V_{DC}
	$R_L \geq 10$ kΩ	27	28		27	28		27	28		27	28		27	28		23	24		V_{DC}
V_{OL}	V^+ = 5 V_{DC}, $R_L \leq 10$ kΩ		5	20		5	20		5	20		5	20		5	20		5	100	mV_{DC}
Output Current																				
Source	V_{IN}^+ = +1 V_{DC}, V_{IN}^- = 0 V_{DC}, V^+ = 15 V_{DC}	10	20		10	20		10	20		10	20		10	20		10	20		mA_{DC}
Sink	V_{IN}^- = +1 V_{DC}, V_{IN}^+ = 0 V_{DC}, V^+ = 15 V_{DC}	10	15		5	8		5	8		5	8		5	8		5	8		mA_{DC}
Differential Input Voltage	(Note 7)			32			32			32			32			32			26	V_{DC}

Note 1: For operating at high temperatures, the LM358/LM358A, LM2904 must be derated based on a +125°C maximum junction temperature and a thermal resistance of 175°C/W which applies for the device soldered in a printed circuit board, operating in a still air ambient. The LM258/LM258A and LM158/LM158A can be derated based on a +150°C maximum junction temperature. The dissipation is the total of all four amplifiers—use external resistors, where possible, to allow the amplifier to saturate or to reduce the power which is dissipated in the integrated circuit.

Note 2: Short circuits from the output to V^+ can cause excessive heating and eventual destruction. The maximum output current is approximately 40 mA independent of the magnitude of V^+. At values of supply voltage in excess of +15 V_{DC}, continuous short-circuits can exceed the power dissipation ratings and cause eventual destruction. Destructive dissipation can result from simultaneous shorts on all amplifiers.

Note 3: This input current will only exist when the voltage at any of the input leads is driven negative. It is due to the collector base junction of the input PNP transistors becoming forward biased and thereby acting as input diode clamps. In addition to this diode action, there is also lateral NPN parasitic transistor action on the IC chip. This transistor action can cause the output voltages of the op amps to go to the V^+ voltage level (or to ground for a large overdrive) for the time duration that an input is driven negative. This is not destructive and normal output states will re-establish when the input voltage, which was negative, again returns to a value greater than −0.3 V_{DC} (at 25°C).

Note 4: These specifications apply for V^+ = +5 V_{DC} and −55°C ≤ T_A ≤ +125°C, unless otherwise stated. With the LM258/LM258A, all temperature specifications are limited to −25°C ≤ T_A ≤ +85°C, the LM358/LM358A temperature specifications are limited to 0°C ≤ T_A ≤ +70°C, and the LM2904 specifications are limited to −40°C ≤ T_A ≤ +85°C.

Note 5: V_O ≅ 1.4 V_{DC}, R_S = 0Ω with V^+ from 5 V_{DC} to 30 V_{DC}; and over the full input common-mode range (0 V_{DC} to V^+ − 1.5 V_{DC}).

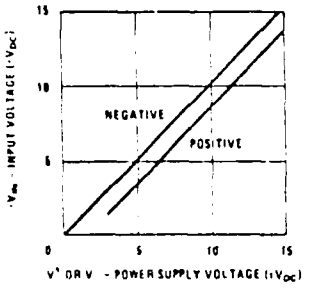
Note 6: The direction of the input current is out of the IC due to the PNP input stage. This current is essentially constant, independent of the state of the output so no loading change exists on the input lines.

Note 7: The input common-mode voltage of either input signal voltage should not be allowed to go negative by more than 0.3V (at 25°C). The upper end of the common-mode voltage range is V^+ −1.5V, but either or both inputs can go to +32 V_{DC} without damage (+26 V_{DC} for LM2904).

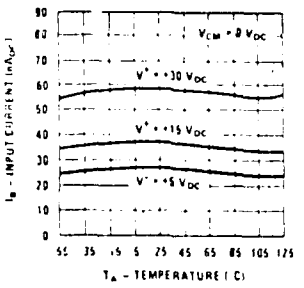
Note 8: Due to proximity of external components, insure that coupling is not originating via stray capacitance between these external parts. This typically can be detected as this type of capacitive increases at higher frequencies.

Typical Performance Characteristics

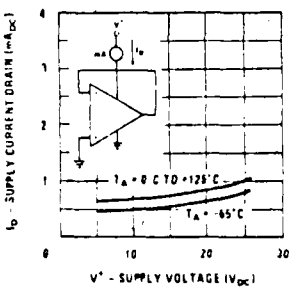
Input Voltage Range



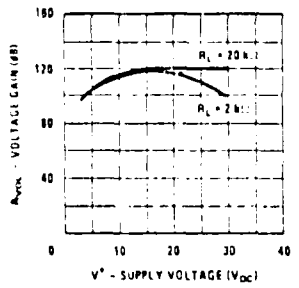
Input Current



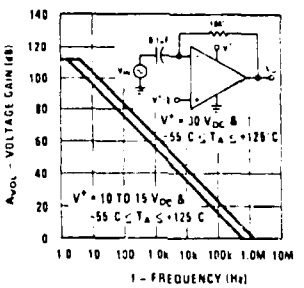
Supply Current



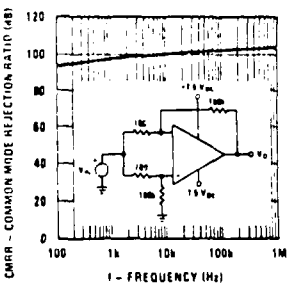
Voltage Gain



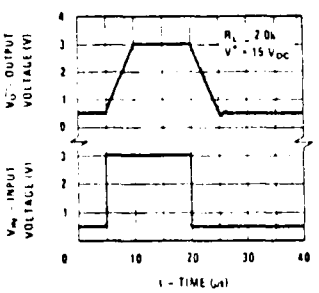
Open Loop Frequency Response



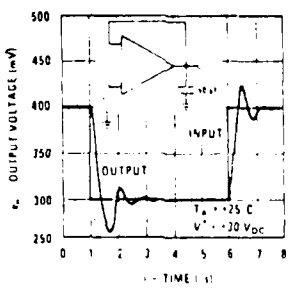
Common Mode Rejection Ratio



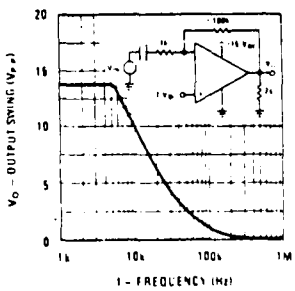
Voltage Follower Pulse Response



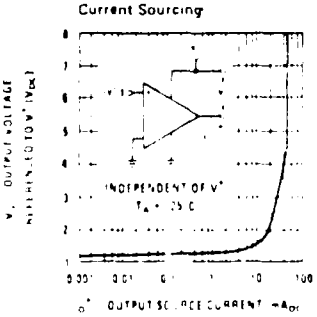
Voltage Follower Pulse Response (Small Signal)



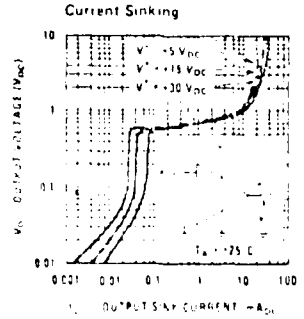
Large Signal Frequency Response



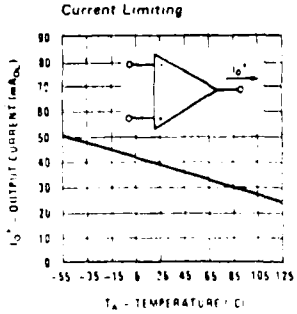
Output Characteristics Current Sourcing



Output Characteristics Current Sinking

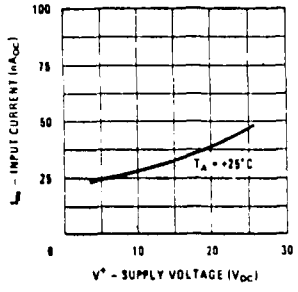


Current Limiting

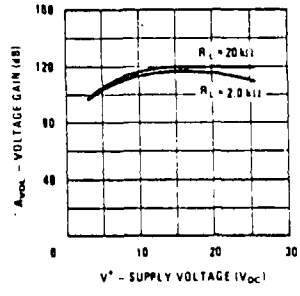


Typical Performance Characteristics (Continued) (LM2902 only)

Input Current



Voltage Gain



Application Hints

The LM158 series are op amps which operate with only a single power supply voltage, have true-differential inputs, and remain in the linear mode with an input common-mode voltage of 0 V_{DC}. These amplifiers operate over a wide range of power supply voltage with little change in performance characteristics. At 25°C amplifier operation is possible down to a minimum supply voltage of 2.3 V_{DC}.

Precautions should be taken to insure that the power supply for the integrated circuit never becomes reversed in polarity or that the unit is not inadvertently installed backwards in a test socket as an unlimited current surge through the resulting forward diode within the IC could cause fusing of the internal conductors and result in a destroyed unit.

Large differential input voltages can be easily accommodated and, as input differential voltage protection diodes are not needed, no large input currents result from large differential input voltages. The differential input voltage may be larger than V^+ without damaging the device. Protection should be provided to prevent the input voltages from going negative more than −0.3 V_{DC} (at 25°C). An input clamp diode with a resistor to the IC input terminal can be used.

To reduce the power supply current drain, the amplifiers have a class A output stage for small signal levels which converts to class B in a large signal mode. This allows the amplifiers to both source and sink large output currents. Therefore both NPN and PNP external current boost transistors can be used to extend the power capability of the basic amplifiers. The output voltage needs to raise approximately 1 diode drop above ground to bias the on-chip vertical PNP transistor for output current sinking applications.

For ac applications, where the load is capacitively coupled to the output of the amplifier, a resistor should be used, from the output of the amplifier to ground to increase the class A bias current and prevent crossover distortion. Where the load is directly coupled, as in dc applications, there is no crossover distortion.

Capacitive loads which are applied directly to the output of the amplifier reduce the loop stability margin. Values of 50 pF can be accommodated using the worst-case non-inverting unity gain connection. Large closed loop gains or resistive isolation should be used if larger load capacitance must be driven by the amplifier.

The bias network of the LM158 establishes a drain current which is independent of the magnitude of the power supply voltage over the range of from 3 V_{DC} to 30 V_{DC}.

Output short circuits either to ground or to the positive power supply should be of short time duration. Units can be destroyed, not as a result of the short circuit current causing metal fusing, but rather due to the large increase in IC chip dissipation which will cause eventual failure due to excessive junction temperatures. Putting direct short-circuits on more than one amplifier at a time will increase the total IC power dissipation to destructive levels, if not properly protected with external dissipation limiting resistors in series with the output leads of the amplifiers. The larger value of output source current which is available at 25°C provides a larger output current capability at elevated temperatures (see typical performance characteristics) than a standard IC op amp.

The circuits presented in the section on typical applications emphasize operation on only a single power supply voltage. If complementary power supplies are available, all of the standard op amp circuits can be used. In general, introducing a pseudo-ground (a bias voltage reference of $V^+/2$) will allow operation above and below this value in single power supply systems. Many application circuits are shown which take advantage of the wide input common-mode voltage range which includes ground. In most cases, input biasing is not required and input voltages which range to ground can easily be accommodated.

National Semiconductor

Operational Amplifiers/Buffers

LM146/LM246/LM346 Programmable Quad Operational Amplifiers

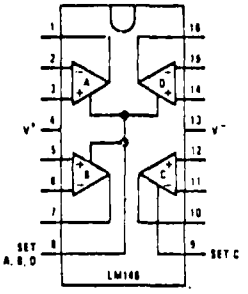
General Description

The LM146 series of quad op amps consists of four independent, high gain, internally compensated, low power, programmable amplifiers. Two external resistors (R_{SET}) allow the user to program the gain bandwidth product, slew rate, supply current, input bias current, input offset current and input noise. For example, the user can trade-off supply current for bandwidth or optimize noise figure for a given source resistance. In a similar way, other amplifier characteristics can be tailored to the application. Except for the two programming pins at the end of the package, the LM146 pin-out is the same as the LM124 and LM148.

Features (I_{SET} = 10 μA)

- Programmable electrical characteristics
- Battery-powered operation
- Low supply current — 350 μA amplifier
- Guaranteed gain bandwidth product — 0.8 MHz min
- Large DC voltage gain — 120 dB
- Low noise voltage — 28 nV/$\sqrt{Hz}$
- Wide power supply range — ±1.5V to ±22V
- Class AB output stage—no crossover distortion
- Ideal pin out for Biquad active filters
- Input bias currents are temperature compensated

Connection Diagrams (Dual-In-Line Packages, Top Views)



Order Number LM146J, LM246J or LM346J
See NS Package J16A

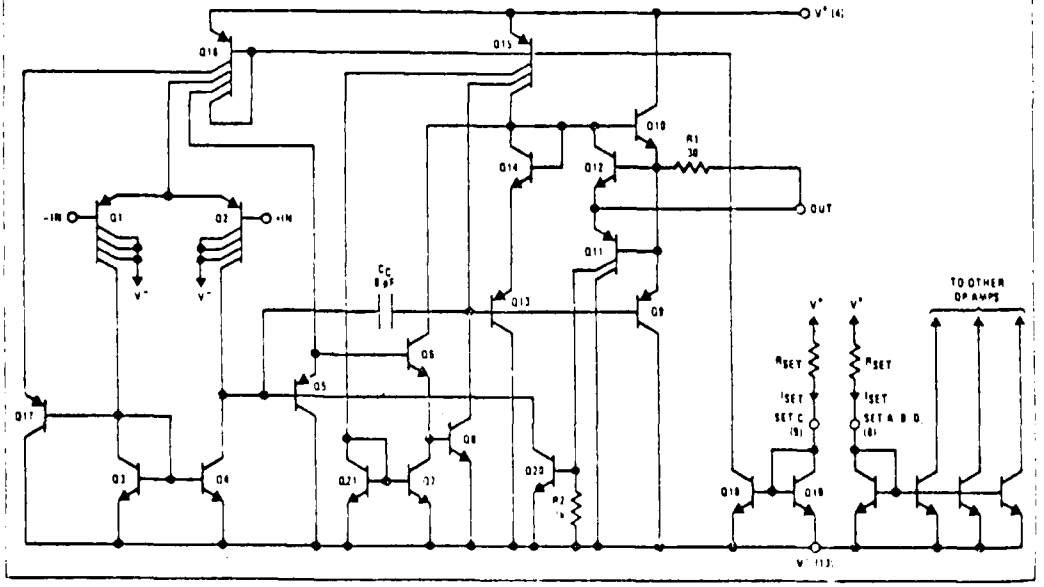
Order Number LM246N or LM346N
See NS Package N16A

PROGRAMMING EQUATIONS

Total Supply Current = 1.4 mA (I_{SET}/10 μA)
Gain Bandwidth Product = 1 MHz (I_{SET}/10 μA)
Slew Rate = 0.4V/μs (I_{SET}/10 μA)
Input Bias Current = 50 nA (I_{SET}/10 μA)
I_{SET} = Current into pin 8, pin 9 (see schematic-diagram)

$$I_{SET} = \frac{V^+ - V^- - 0.6V}{R_{SET}}$$

Schematic Diagram



Absolute Maximum Ratings (Note 1)

	LM146	LM246	LM346
Supply Voltage	±22V	±18V	±18V
Differential Input Voltage (Note 1)	±30V	±30V	±30V
CM Input Voltage (Note 1)	±15V	±15V	±15V
Power Dissipation (Note 2)	900 mW	500 mW	500 mW
Output Short-Circuit Duration (Note 3)	Indefinite	Indefinite	Indefinite
Operating Temperature Range	−55°C to +125°C	−25°C to +85°C	0°C to +70°C
Maximum Junction Temperature	150°C	110°C	100°C
Storage Temperature Range	−65°C to +150°C	−65°C to +150°C	−65°C to +150°C
Lead Temperature (Soldering, 10 seconds)	300°C	300°C	300°C
Thermal Resistance (θ_{jA}), (Note 2)			
Cavity DIP (D) (J) P_d	900 mW	900 mW	900 mW
θ_{jA}	90°C/W	90°C/W	90°C/W
Molded DIP (N) P_d			500 mW
θ_{jA}			140°C/W

DC Electrical Characteristics (V_S = ±15V, I_{SET} = 10 μA, Note 4)

PARAMETER	CONDITIONS	LM146			LM246/LM346			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
Input Offset Voltage	V_{CM} = 0V, $R_S \leq 50\ \Omega$, T_A = 25°C		0.5	5		0.5	6	mV
Input Offset Current	V_{CM} = 0V, T_A = 25°C		2	20		2	100	nA
Input Bias Current	V_{CM} = 0V, T_A = 25°C		50	100		50	250	nA
Supply Current (4 Op Amps)	T_A = 25°C		1.4	2.0		1.4	2.5	mA
Large Signal Voltage Gain	R_L = 10 kΩ, ΔV_{OUT} = ±10V, T_A = 25°C	100	1000		50	1000		V/mV
Input CM Range	T_A = 25°C	±13.5	±14		±13.5	±14		V
CM Rejection Ratio	$R_S \leq 10$ kΩ, T_A = 25°C	80	100		70	100		dB
Power Supply Rejection Ratio	$R_S \leq 10$ kΩ, T_A = 25°C	80	100		74	100		dB
Output Voltage Swing	$R_L \geq 10$ kΩ, T_A = 25°C	±12	±14		±12	±14		V
Short Circuit Current	T_A = 25°C	5	20	35	5	20	35	mA
Gain Bandwidth Product	T_A = 25°C	0.8	1.2		0.5	1.2		MHz
Phase Margin	T_A = 25°C		60			60		Deg
Slew Rate	T_A = 25°C		0.4			0.4		V/μs
Input Noise Voltage	f = 1 kHz, T_A = 25°C		28			28		$nV/\sqrt{Hz}$
Channel Separation	R_L = 10 kΩ, ΔV_{OUT} = 0V to ±12V, T_A = 25°C		120			120		dB
Input Resistance	T_A = 25°C		1.0			1.0		MΩ
Input Capacitance	T_A = 25°C		2.0			2.0		pF
Input Offset Voltage	V_{CM} = 0V, $R_S \leq 50\ \Omega$		0.5	6		0.5	7.5	mV
Input Offset Current	V_{CM} = 0V		2	25		2	100	nA
Input Bias Current	V_{CM} = 0V		50	100		50	250	nA
Supply Current (4 Op Amps)			1.5	2.0		1.5	2.5	mA
Large Signal Voltage Gain	R_L = 10 kΩ, ΔV_{OUT} = ±10V	50	1000		25	1000		V/mV
Input CM Range		±13.5	±14		±13.5	±14		V
CM Rejection Ratio	$R_S \leq 50\ \Omega$	70	100		70	100		dB
Power Supply Rejection Ratio	$R_S \leq 50\ \Omega$	76	100		74	100		dB
Output Voltage Swing	$R_L \geq 10$ kΩ	±12	±14		±12	±14		V

DC Electrical Characteristics (V_S = ±15V, I_{SET} = 1 μA)

PARAMETER	CONDITIONS	LM146			LM246/LM346			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
Input Offset Voltage	V_{CM} = 0V, $R_S \leq 50\,\Omega$, T_A = 25°C		0.5	5		0.5	7	mV
Input Bias Current	V_{CM} = 0V, T_A = 25°C		7.5	20		7.5	100	nA
Supply Current (4 Op Amps)	T_A = 25°C		140	250		140	300	μA
Gain Bandwidth Product	T_A = 25°C	80	100		50	100		kHz

DC Electrical Characteristics (V_S = ±1.5V, I_{SET} = 10 μA)

PARAMETER	CONDITIONS	LM146			LM246/LM346			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
Input Offset Voltage	V_{CM} = 0V, $R_S \leq 50\,\Omega$, T_A = 25°C		0.5	5		0.5	7	mV
Input CM Range	T_A = 25°C	+0.7			±0.7			V
CM Rejection Ratio	$R_S \leq 50\,\Omega$, T_A = 25°C		80			80		dB
Output Voltage Swing	$R_L \geq 10\,k\Omega$, T_A = 25°C	±0.6			±0.6			V

Note 1: For supply voltages less than ±15V, the absolute maximum input voltage is equal to the supply voltage.

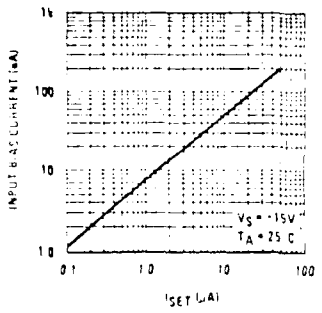
Note 2: The maximum power dissipation for these devices must be derated at elevated temperatures and is dictated by T_{JMAX}, θ_{JA}, and the ambient temperature, T_A. The maximum available power dissipation at any temperature is $P_D = (T_{JMAX} - T_A)/\theta_{JA}$ or the 25°C P_{DMAX}, whichever is less.

Note 3: Any of the amplifier outputs can be shorted to ground indefinitely; however, more than one should not be simultaneously shorted as the maximum junction temperature will be exceeded.

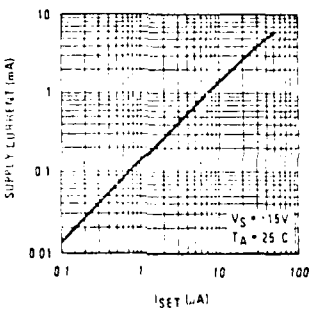
Note 4: These specifications apply over the absolute maximum operating temperature range unless otherwise noted.

Typical Performance Characteristics

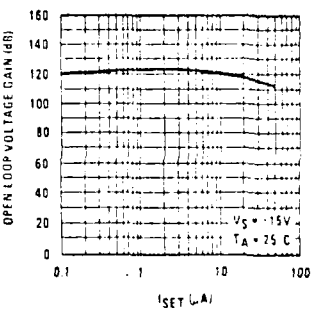
Input Bias Current vs I_{SET}



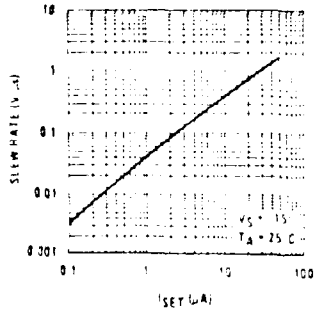
Supply Current vs I_{SET}



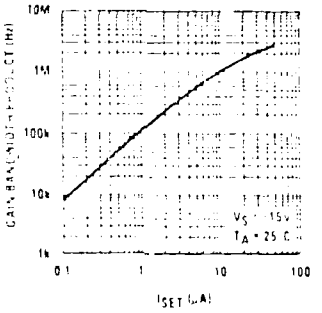
Open Loop Voltage Gain vs I_{SET}



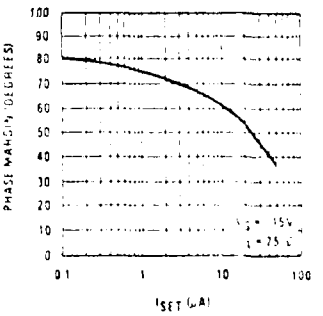
Slew Rate vs I_{SET}



Gain Bandwidth Product vs I_{SET}



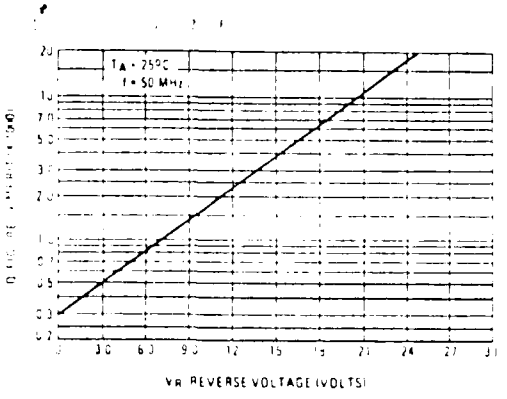
Phase Margin vs I_{SET}

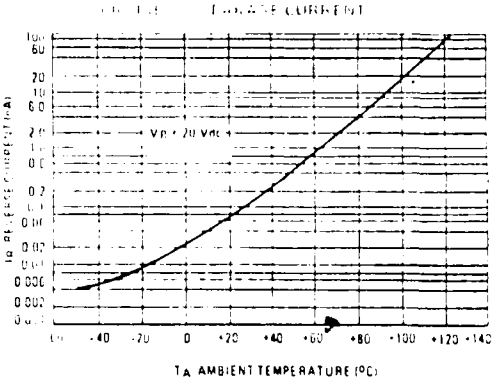


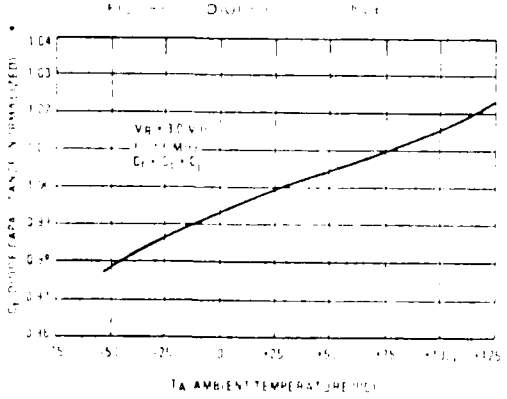
ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	Min	Typ	Max	Unit
Reverse Breakdown Voltage (I_R = 10 μAdc)	BV_R	30	-	-	Vdc
Reverse Voltage Leakage Current (V_R = 25 Vdc)	I_R		-	0.1	μAdc
Series Inductance (Note 1) (f = 250 MHz, Lead Length ≤ 1.8)	L_S		6.0	-	nH
Case Capacitance (Note 2) (f = 1.0 MHz)	C_C		0.2	-	pF
Diode Capacitance Temperature Coefficient (V_R = 3.0 Vdc, f = 1.0 MHz)	TC_C	-	300	400	ppm/°C

Device	C_t, Diode Capacitance V_R = 3.0 Vdc, f = 1.0 MHz pF			Q, Figure of Merit V_R = 3.0 Vdc f = 50 MHz (Note 3)	C_R, Capacitance Ratio C_3/C_{25} f = 1.0 MHz (Note 4)	
	Min	Nom	Max	Min	Min	Max
MV209	26	29	32	200	5.0	6.5







NOTES ON TESTING AND SPECIFICATIONS

1. L_S is measured on a package having a short instead of a die, using an impedance bridge (Boonton Radio Model 250A RX Meter).
2. C_C is measured on a package without a die, using a capacitance bridge (Boonton Electronics Model 75A or equivalent).
3. Q is calculated by taking the G and C readings of an admittance bridge, such as Boonton Electronics Model 33AS8, at the specified frequency and substituting in the following equation:

$$Q = \frac{2\pi fC}{G}$$

4. C_R is the ratio of C_t measured at 3.0 Vdc divided by C_t measured at 25 Vdc.

MOTOROLA
Semiconductors
BOX 20912 • PHOENIX, ARIZONA 85036

MV209

VVC

SILICON EPICAP▲ DIODE

designed for VHF TV tuning, AFC, general frequency control and tuning applications; providing solid-state reliability in replacement of mechanical tuning methods.

- High Q With Guaranteed Minimum Values at VHF Frequencies
- Controlled and Uniform Tuning Ratio
- Guaranteed Matching[1] Tolerance From Diode to Diode and Group to Group
- Supplied in One-Piece, Unibloc▲ Package for High Reliability

[1] Upon request, diodes are available in matched sets of any number or in matched groups. All diodes in a set or group can be matched for capacitance to ±3% or 0.1 pF (whichever is greater) along the entire specified tuning range.

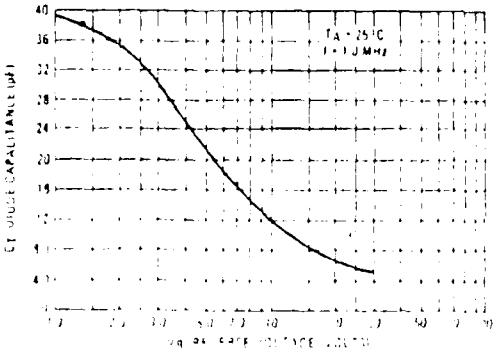
VOLTAGE VARIABLE CAPACITANCE DIODE

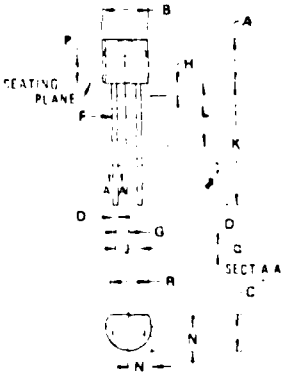
26-32 pF

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Reverse Voltage	V_R	30	Volts
Forward Current	I_F	200	mA
Power Dissipation @ T_A = 25°C	P_D	280	mW
Derate above 25°C		2.8	mW/°C
Junction Temperature	T_J	+125	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

FIGURE 1 – DIODE CAPACITANCE





STYLE 2:
PIN 1 CATHODE
2 ANODE

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	4.32	5.33	0.170	0.210
B	4.45	5.21	0.175	0.205
C	3.18	4.19	0.125	0.165
D	0.406	0.533	0.016	0.021
F	0.107	0.482	0.015	0.019
G	1.27 BSC		0.050 BSC	
H		1.27		0.050
J	2.54 BSC		0.100 BSC	
K	12.70		0.500	
L	6.35		0.250	
N	2.41	2.66	0.095	0.105
P	3.81		0.150	
R	1.43		0.135	

CASE 182-02

▲Trademark of Motorola Inc.

MOTOROLA INC. 1973

DS 8548

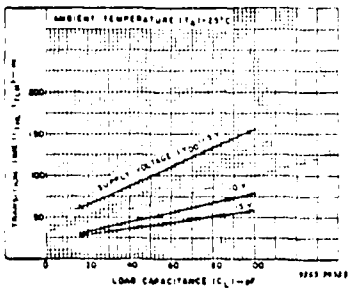


Fig. 12 – Typical transition time vs. load capacitance.

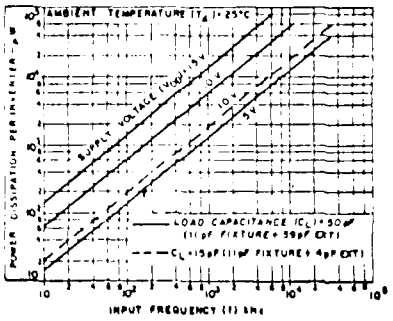


Fig. 13 – Typical dynamic power dissipation vs. frequency.

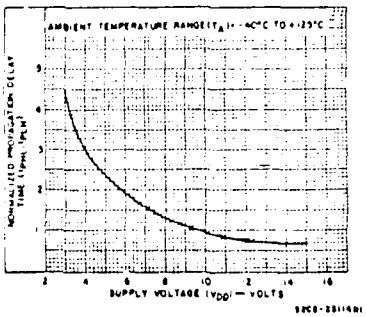


Fig. 14 – Variation of normalized propagation delay time (t_{PHL} and t_{PLH}) with supply voltage.

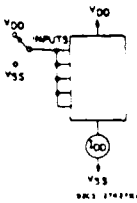


Fig. 15 – Quiescent device current test circuit.

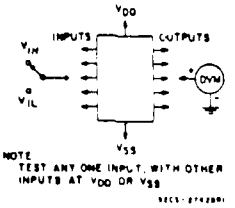


Fig. 16 – Noise immunity test circuit.

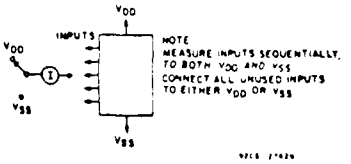


Fig. 17 – Input leakage current test circuit.

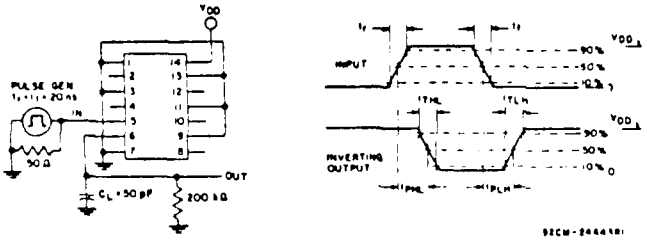


Fig. 18 – Dynamic electrical characteristics test circuit and waveforms.

APPLICATIONS

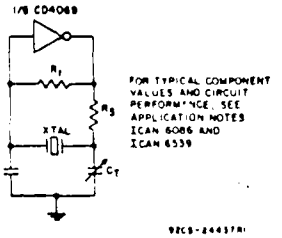


Fig. 19 – Typical crystal oscillator circuit.

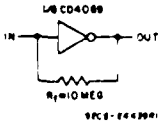


Fig. 20 – High-input impedance amplifier.

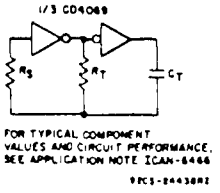
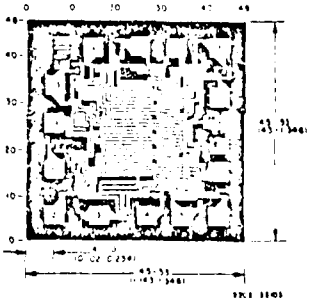


Fig. 21 – Typical RC oscillator circuit.



Dimensions and pad layout for CD4069UBH

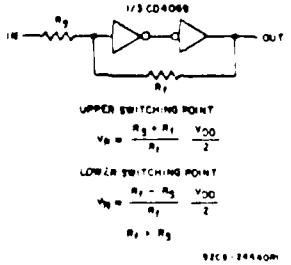


Fig. 22 – Input pulse shaping circuit (Schmitt trigger)

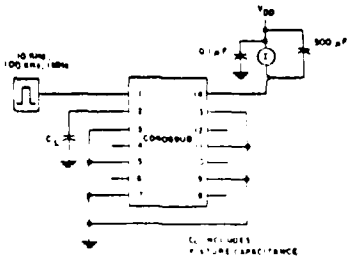


Fig. 23 – Dynamic power dissipation test circuit.

Dimensions in parentheses are in millimeters and are derived from the basic inch dimensions as indicated. Grid graduations are in mils (10^{-3} inch).

The photographs and dimensions of each CMOS chip represent a chip when it is part of the wafer. When the wafer is separated into individual chips, the angle of cleavage may vary with respect to the chip face for different chips. The actual dimensions of the isolated chip therefore may differ slightly from the nominal dimensions shown. The user should consider a tolerance of −3 mils to +16 mils applicable to the nominal dimensions shown.

STATIC ELECTRICAL CHARACTERISTICS

CHARACTERISTIC	CONDITIONS			LIMITS AT INDICATED TEMPERATURES (°C) Values at −55, +25, +125 Apply to D,F,K,H Packages Values at −40, +25, +85 Apply to E Package							UNITS
	V_O (V)	V_{IN} (V)	V_{DD} (V)	−55	−40	+85	+125	+25 Min.	+25 Typ.	+25 Max.	
Quiescent Device Current, I_{DD} Max	–	0,5	5	0.25	0.25	7.5	7.5	–	0.01	0.25	μA
	–	0,10	10	0.5	0.5	15	15	–	0.01	0.5	
	–	0,15	15	1	1	30	30	–	0.01	1	
	–	0,20	20	5	5	150	150	–	0.02	5	
Output Low (Sink) Current I_{OL} Min	0.4	0,5	5	0.64	0.61	0.42	0.36	0.51	1	–	mA
	0.5	0,10	10	1.6	1.5	1.1	0.9	1.3	2.6	–	
	1.5	0,15	15	4.2	4	2.8	2.4	3.4	6.8	–	
Output High (Source) Current, I_{OH} Min	4.6	0,5	5	−0.64	−0.61	−0.42	−0.36	−0.51	−1	–	
	2.5	0,5	5	−2	−1.8	−1.3	−1.15	−1.6	−3.2	–	
	9.5	0,10	10	−1.6	−1.5	−1.1	−0.9	−1.3	−2.6	–	
	13.5	0,15	15	−4.2	−4	−2.8	−2.4	−3.4	−6.8	–	
Output Voltage Low Level, V_{OL} Max	–	5	5	0.05				–	0	0.05	V
	–	10	10	0.05				–	0	0.05	
	–	15	15	0.05				–	0	0.05	
Output Voltage High Level V_{OH} Min	–	0	5	4.95				4.95	5	–	
	–	0	10	9.95				9.95	10	–	
	–	0	15	14.95				14.95	15	–	
Input Low Voltage, V_{IL} Max	4.5	–	5	1				–	–	1	V
	9	–	10	2				–	–	2	
	13.5	–	15	2.5				–	–	2.5	
Input High Voltage, V_{IH} Min	0.5	–	5	4				4	–	–	
	1	–	10	8				8	–	–	
	1.5	–	15	12.5				12.5	–	–	
Input Current I_{IN} Max		0,18	18	±0.1	±0.1	±1	±1	–	$±10^{-5}$	±0.1	μA

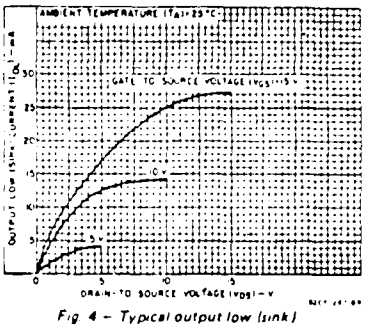


Fig. 4 – Typical output low (sink) current characteristics.

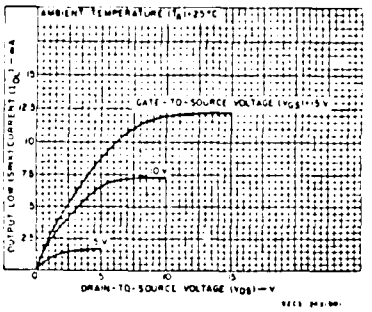


Fig. 5 – Minimum output low (sink) current characteristics.

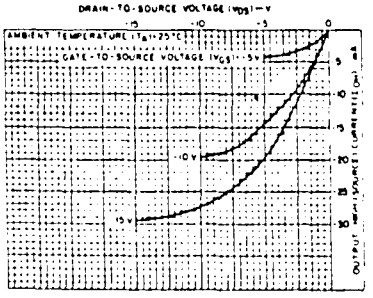


Fig. 8 – Typical output high (source) current characteristics.

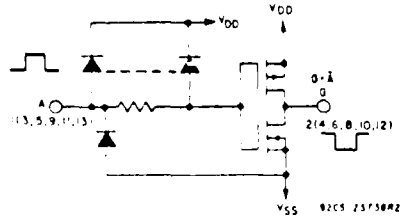


Fig. 6 – Schematic diagram of one of six identical inverters.

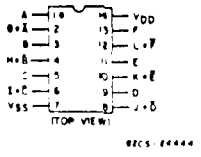


Fig. 7 – CD4069UB terminal assignment.

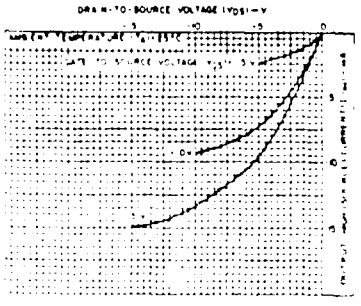


Fig. 9 – Minimum output high (source) current characteristics.

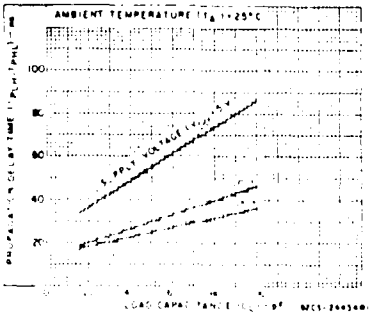


Fig. 10 – Typical propagation delay time vs load capacitance.

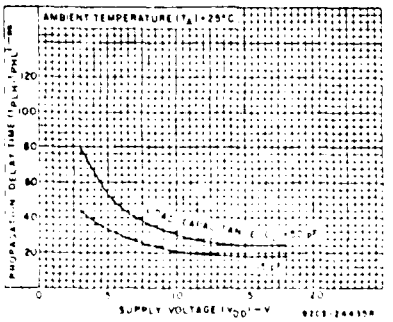


Fig. 11 – Typical propagation delay time vs supply voltage.

CD4069UB Types

CMOS Hex Inverter

High-Voltage Types (20-Volt Rating)

The RCA-CD4069UB types consist of six CMOS inverter circuits. These devices are intended for all general purpose inverter applications where the medium power TTL drive and logic level conversion capabilities of circuits such as the CD4009 and CD4049 Hex Inverter Buffers are not required.

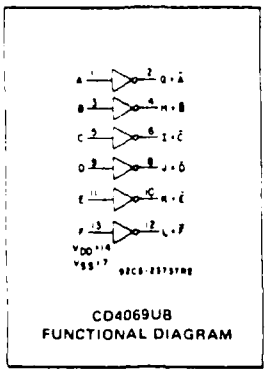
The CD4069UB-Series types are supplied in 14-lead hermetic dual-in-line ceramic packages (D and F suffixes), 14-lead dual-in-line plastic package (E suffix), 14-lead ceramic flat package (K suffix), and in chip form (H suffix).

Features

- Standardized symmetrical output characteristics
- Medium Speed Operation—t_{PHL}, t_{PLH}=30 ns (typ.) at 10 V
- 100% tested for quiescent current at 20 V
- Maximum input current of 1 μA at 18 V over full package-temperature range; 100 nA at 18 V and 25°C
- Meets all requirements of JEDEC Tentative Standard No. 13A, "Standard Specifications for Description of 'B' Series CMOS Devices"

Applications:

- Logic inversion
- Pulse shaping
- Oscillators
- High-input-impedance amplifiers



CD4069UB
FUNCTIONAL DIAGRAM

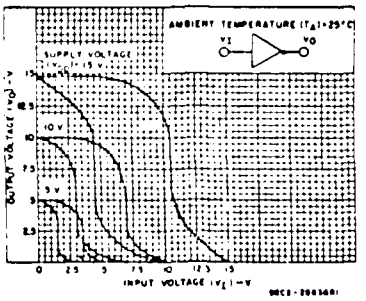


Fig. 1 – Minimum and maximum voltage transfer characteristics.

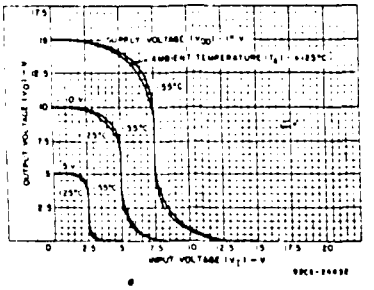


Fig. 2 – Typical voltage transfer characteristics as a function of temperature.

RECOMMENDED OPERATING CONDITIONS

For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	LIMITS		UNITS
	Min.	Max.	
Supply Voltage Range (For T_A = Full Package Temperature Range)	3	18	V

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY-VOLTAGE RANGE, (V_{DD})
(Voltages referenced to V_{SS} Terminal) . . . . . −0.5 to +20 V
INPUT VOLTAGE RANGE, ALL INPUTS . . . . . −0.5 to V_{DD} +0.5 V
DC INPUT CURRENT, ANY ONE INPUT . . . . . ±10 mA
POWER DISSIPATION PER PACKAGE (P_D):
For T_A = −40 to +60°C (PACKAGE TYPE E) . . . . . 500 mW
For T_A = +60 to +85°C (PACKAGE TYPE E) . . . . . Derate Linearly at 12 mW/°C to 200 mW
For T_A = −55 to +100°C (PACKAGE TYPES D, F, K) . . . . . 500 mW
For T_A = +100 to +125°C (PACKAGE TYPES D, F, K) . . . . . Derate Linearly at 12 mW/°C to 200 mW
DEVICE DISSIPATION PER OUTPUT TRANSISTOR
FOR T_A = FULL PACKAGE-TEMPERATURE RANGE (All Package Types) . . . . . 100 mW
OPERATING-TEMPERATURE RANGE (T_A):
PACKAGE TYPES D, F, K, H . . . . . −55 to +125°C
PACKAGE TYPE E . . . . . −40 to +85°C
STORAGE TEMPERATURE RANGE (T_{stg}) . . . . . −65 to +150°C
LEAD TEMPERATURE (DURING SOLDERING)
At distance 1/16 ± 1/32 inch (1.59 ± 0.79 mm) from case for 10 s max. . . . . +265°C

DYNAMIC ELECTRICAL CHARACTERISTICS at T_A = 25°C; Input t_r, t_f = 20 ns, C_L = 50 pF, R_L = 200 KΩ

CHARACTERISTIC		CONDITIONS V_{DD} V	ALL TYPES LIMITS Typ.	Max.	UNITS
Propagation Delay Time,	t_{PLH}, t_{PHL}	5	55	110	ns
		10	30	60	
		15	25	50	
Transition Time,	t_{THL}, t_{TLH}	5	100	200	ns
		10	50	100	
		15	40	80	
Input Capacitance,	C_{IN}	Any Input	10	15	pF

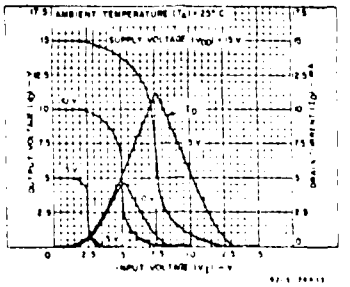


Fig. 3 – Typical current and voltage transfer characteristics.

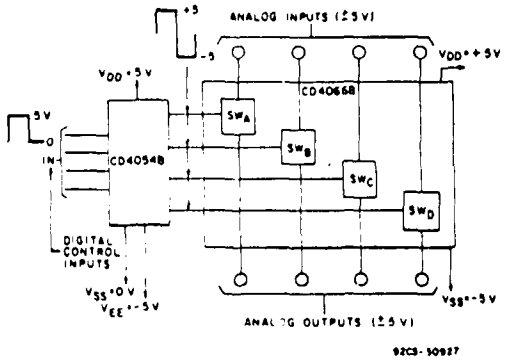
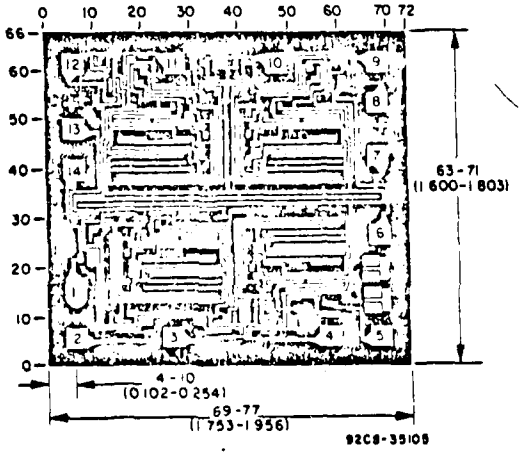


Fig. 18 – Bidirectional signal transmission via digital control logic.



CD4066BH
CHIP PHOTOGRAPH

Dimensions in parentheses are in millimeters and are derived from the basic inch dimensions as indicated. Grid graduations are in mils (10^{-3} inch).

The photographs and dimensions of each CMOS chip represent a chip when it is part of the wafer. When the wafer is separated into individual chips, the angle of cleavage may vary with respect to the chip face for different chips. The actual dimensions of the isolated chip, therefore, may differ slightly from the nominal dimensions shown. The user should consider a tolerance of −3 mils to +16 mils applicable to the nominal dimensions shown.

SPECIAL CONSIDERATIONS — CD4066B

1. In applications that employ separate power sources to drive V_{DD} and the signal inputs, the V_{DD} current capability should exceed V_{DD}/R_L (R_L = effective external load of the four CD4066B bilateral switches). This provision avoids any permanent current flow or clamp action on the V_{DD} supply when power is applied or removed from the CD4066B.
2. In certain applications, the external load-resistor current may include both V_{DD} and signal-line components. To avoid drawing V_{DD} current when switch current flows into terminals 1,4,8, or 11, the voltage drop across the bidirectional switch must not exceed 0.8 volts (calculated from R_{ON} values shown).

   No V_{DD} current will flow through R_L if the switch current flows into terminals 2,3,9, or 10.

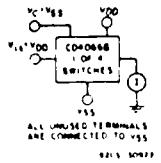


Fig. 11 – Off-switch input or output leakage.

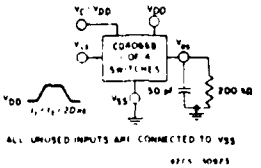


Fig. 12 – Propagation delay time signal input (V_{is}) to signal output (V_{os}).

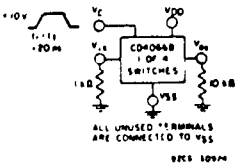


Fig. 13 – Crosstalk-control input to signal output.

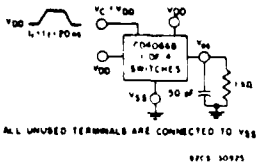


Fig. 14 – Propagation delay t_{PLH}, t_{PHL} control-signal output. Delay is measured at V_{os} level of +10% from ground (turn-on) or on-state output level (turn-off).

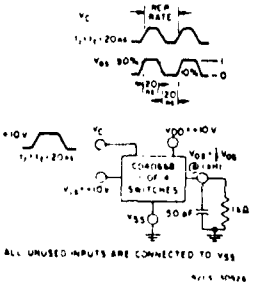


Fig. 15 – Maximum allowable control input repetition rate.

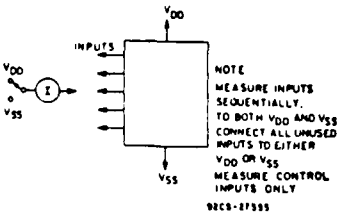


Fig. 16 – Input leakage current test circuit.

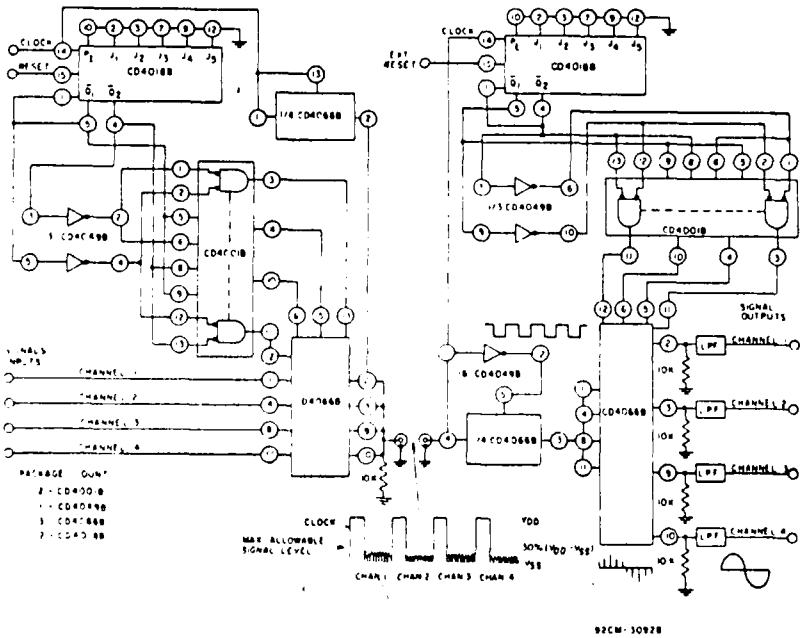


Fig. 17– 4-channel PAM multiplex system diagram.

ELECTRICAL CHARACTERISTICS (cont'd)

Characteristic	Test Conditions	V_{DD} (V)	LIMITS AT INDICATED TEMPERATURES (°C) Values at -55, +25, +125 Apply to D, F, K, H, Packages Values at −40, +25, +85 Apply to E Package						UNITS
			−55	−40	+85	+125	+25 Typ.	+25 Max.	
Control (V_C)									
Control Input Low Voltage, V_{ILC} Max.	$\lvert I_{is}\rvert < 10\,\mu A$ $V_{is} = V_{SS}, V_{OS} = V_{DD}$ and $V_{is} = V_{DD}, V_{OS} = V_{SS}$	5	1	1	1	1	–	1	V
		10	2	2	2	2	–	2	
		15	2	2	2	2	–	2	
Control Input High Voltage, V_{IHC}	See Fig. 6	5	3.5 (Min.)						V
		10	7 (Min.)						
		15	11 (Min.)						
Input Current, I_{IN} Max.	$V_{is} \leq V_{DD}$ $V_{DD} - V_{SS} = 18$ V $V_{CC} \leq V_{DD} - V_{SS}$	18	±0.1	±0.1	±1	±1	±10^{-5}	±0.1	μA
Crosstalk (Control Input to Signal Output)	V_C = 10 V (Sq. Wave) t_r, t_f = 20 ns R_L = 10 kΩ	10	–	–	–	–	50	–	mV
Turn-On and Turn-Off Propagation Delay	$V_{IN} = V_{DD}$ t_r, t_f = 20 ns C_L = 50 pF R_L = 1 kΩ	5	–	–	–	–	35	70	ns
		10	–	–	–	–	20	40	
		15	–	–	–	–	15	30	
Maximum Control Input Repetition Rate	$V_{is} = V_{DD}$, V_{SS} = GND, R_L = 1 kΩ to gnd, C_L = 50 pF, V_C = 10 V(Square wave centered on 5 V) t_r, t_f = 20 ns, V_{os} = ½ V_{os} @ 1 kHz	5	–	–	–	–	6	–	MHz
		10	–	–	–	–	9	–	
		15	–	–	–	–	9.5	–	
Input Capacitance, C_{IN}			–	–	–	–	5	7.5	μF

V_{DD} (V)	V_{is} (V)	Switch Input I_{is} (mA) −55°C	−40°C	+25°C	+85°C	+125°C	Switch Output, V_{os} (V) Min.	Max.
5	0	0.64	0.61	0.51	0.42	0.36	–	0.4
5	5	−0.64	−0.61	−0.51	−0.42	−0.36	4.6	–
10	0	1.6	1.5	1.3	1.1	0.9	–	0.5
10	10	−1.6	−1.5	−1.3	−1.1	−0.9	9.5	–
15	0	4.2	4	3.4	2.8	2.4	–	1.5
15	15	−4.2	−4	−3.4	−2.8	−2.4	13.5	–

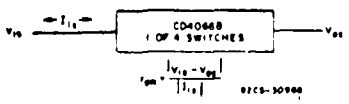


Fig. 6— Determination of r_{on} as a test condition for control input high voltage (V_{IHC}) specification.

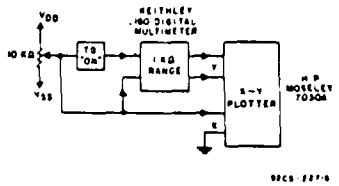


Fig. 7 – Channel on-state resistance measurement circuit.

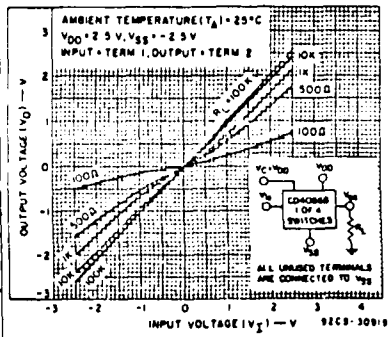


Fig. 8—Typical ON characteristics for 1 of 4 Channels.

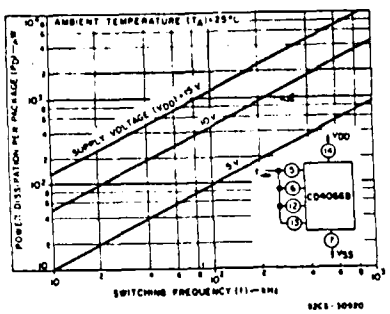


Fig. 9 – Power dissipation per package vs. switching frequency.

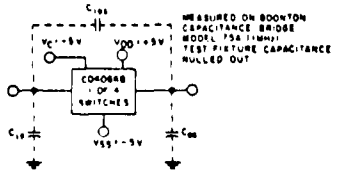


Fig. 10 – Capacitance test circuit.

ELECTRICAL CHARACTERISTICS

Characteristic	Test Conditions	V_{IN} (V)	V_{DD} (V)	LIMITS AT INDICATED TEMPERATURES (°C) Values at -55, +25, +125 Apply to D, F, K, H Packages Values at -40, +25, +85 Apply to E Package				+25		UNITS
				-55	-40	+85	+125	Typ.	Max.	
Quiescent Device Current, I_{DD}		0,5	5	0.25	0.25	7.5	7.5	0.01	0.25	μA
		0,10	10	0.5	0.5	15	15	0.01	0.5	
		0,15	15	1	1	30	30	0.01	1	
		0,20	20	5	5	150	150	0.02	5	
Signal Inputs (V_{is}) and Output (V_{os})										
On-State Resistance, r_{on} Max	$V_C = V_{DD}$, R_L = 10 kΩ returned to $\frac{V_{DD} - V_{SS}}{2}$, $V_{is} = V_{SS}$ to V_{DD}		5	800	850	1200	1300	470	1050	Ω
			10	310	330	500	550	180	400	
			15	200	210	300	320	125	240	
ΔOn-State Resistance Between Any 2 Switches, Δr_{on}	R_L = 10 kΩ, $V_C = V_{DD}$		5	–	–	–	–	15	–	Ω
			10	–	–	–	–	10	–	
			15	–	–	–	–	5	–	
Total Harmonic Distortion, THD	$V_C = V_{DD}$ = 5 V, V_{SS} = -5 V, $V_{is(p-p)}$ = 5 V (Sine wave centered on 0 V) R_L = 10 kΩ, f_{is} = 1 kHz sine wave			–	–	–	–	0.4	–	%
-3dB Cutoff Frequency (Switch on)	$V_C = V_{DD}$ = 5 V, V_{SS} = -5 V, $V_{is(p-p)}$ = 5 V (Sine wave centered on 0 V R_L = 1 kΩ,			–	–	–	–	40	–	MHz
-50dB Feedthrough Frequency (Switch off)	$V_C = V_{SS}$ = -5 V, $V_{is(p-p)}$ = 5 V Sine wave centerd on 0 V R_L = 1 kΩ			–	–	–	–	1	–	MHz
Input/Output Leakage Current (Switch off) I_{is} Max.	V_C = 0 V V_{is} = 18 V, V_{os} = 0 V, V_{is} = 0V, V_{os} = 18 V		18	±0.1	±0.1	±1	±1	$±10^{-5}$	±0.1	μA
-50 dB Crosstalk Frequency	V_C(A) = V_{DD} = +5 V, V_C(B) = V_{SS} = -5 V, V_{is}(A) = 5 V_{p-p}, 50 Ω source R_L = 1 kΩ			–	–	–	–	8	–	MHz
Propagation Delay (Signal Input to Signal Output) t_{pd}	R_L = 200 kΩ $V_C = V_{DD}$, V_{SS} = GND, C_L = 50 pF V_{is} = 10 V (Square wave centered on 5 V t_r, t_f = 20 ns		5	–	–	–	–	20	40	ns
			10	–	–	–	–	10	20	
			15	–	–	–	–	7	15	
Capacitance Input, C_{is}	V_{DD} = +5 V $V_C = V_{SS}$ = -5 V			–	–	–	–	8	–	pF
Output, C_{os}				–	–	–	–	8	–	
Feedthrough, C_{ios}				–	–	–	–	0.5	–	

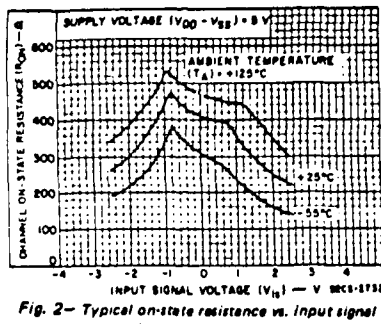


Fig. 2– Typical on-state resistance vs. input signal voltage (all types).

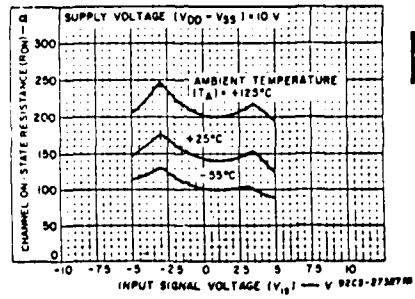


Fig. 3– Typical on-state vs. input signal voltage (all types).

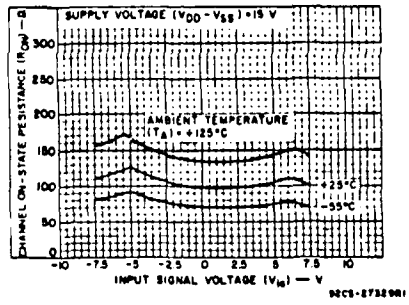


Fig. 4– Typical on-state resistance vs. input signal voltage (all types).

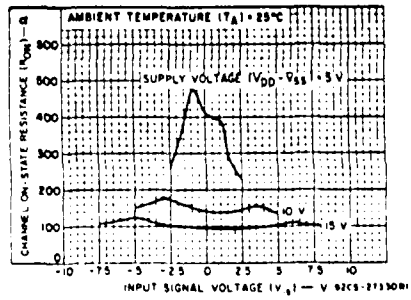


Fig. 5– on-state resistance vs. input signal voltage (all types).

CMOS Quad Bilateral Switch

For Transmission or Multiplexing of Analog or Digital Signals

High-Voltage Types (20-Volt Rating)

The RCA-CD4066B is a quad bilateral switch intended for the transmission or multiplexing of analog or digital signals. It is pin-for-pin compatible with RCA-CD4016B, but exhibits a much lower on-state resistance. In addition, the on-state resistance is relatively constant over the full input-signal range.

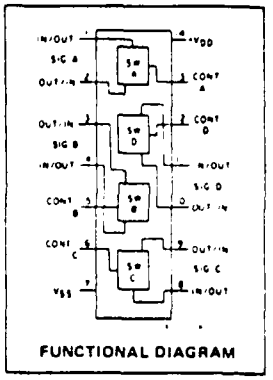
The CD4066B consists of four independent bilateral switches. A single control signal is required per switch. Both the p and the n device in a given switch are biased on or off simultaneously by the control signal. As shown in Fig.1, the well of the n-channel device on each switch is either tied to the input when the switch is on or to V_{SS} when the switch is off. This configuration eliminates the variation of the switch-transistor threshold voltage with input signal, and thus keeps the on-state resistance low over the full operating-signal range.

The advantages over single-channel switches include peak input-signal voltage swings equal to the full supply voltage, and more constant on-state impedance over the input-signal range. For sample-and-hold applications, however, the CD4016B is recommended.

The CD4066B is available in 14-lead ceramic dual-in-line packages (D and F suffixes), 14-lead plastic dual-in-line packages (E suffix), 14-lead ceramic flat packages (K suffix), and in chip form (H suffix).

Features:

- 15-V digital or ±7.5-V peak-to-peak switching
- 125Ω typical on-state resistance for 15-V operation
- Switch on-state resistance matched to within 5 Ω over 15-V signal-input range
- On-state resistance flat over full peak-to-peak signal range
- High on/off output-voltage ratio: 80 dB typ. @ f_{is} = 10 kHz, R_L = 1 kΩ
- High degree of linearity: <0.5% distortion typ. @ f_{is} = 1 kHz, V_{is} = 5 Vp-p, $V_{DD} - V_{SS} \geq 10$ V, R_L = 10 kΩ
- Extremely low off-state switch leakage resulting in very low offset current and high effective off-state resistance: 10 pA typ. @ $V_{DD} - V_{SS}$ = 10 V, T_A = 25°C
- Extremely high control input impedance (control circuit isolated from signal circuit): 10^{12} Ω typ.
- Low crosstalk between switches: −50 dB typ. @ f_{is} = 8 MHz, R_L = 1 kΩ
- Matched control-input to signal-output capacitance: Reduces output signal transients
- Frequency response, switch on = 40 MHz (typ.)
- 100% tested for quiescent current at 20 V
- 5-V, 10-V, and 15-V parametric ratings
- Meets all requirements of JEDEC Tentative Standard No.13A, "Standard Specifications for Description of "B" Series CMOS Devices"



FUNCTIONAL DIAGRAM

Applications:

- Analog signal switching/multiplexing
  - Signal gating
  - Squelch control
  - Chopper
  - Modulator
  - Demodulator
  - Commutating switch
- Digital signal switching/Multiplexing
- Transmission-gate logic implementation
- Analog-to-digital & digital-to-analog conversion
- Digital control of frequency, impedance, phase, and analog-signal gain

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY-VOLTAGE RANGE, (V_{DD}) (Voltages referenced to V_{SS} Terminal)	−0.5 to +20 V
INPUT VOLTAGE RANGE, ALL INPUTS	−0.5 to V_{DD} +0.5 V
DC INPUT CURRENT, ANY ONE INPUT (except for TRANSMISSION GATE which is 25 mA)	±10 mA
POWER DISSIPATION PER PACKAGE (P_D)	
For T_A = −40 to +60°C (PACKAGE TYPE E)	500 mW
For T_A = +60 to +85°C (PACKAGE TYPE E)	Derate Linearly at 12 mW/°C to 200 mW
For T_A = −55 to +100°C (PACKAGE TYPES D, F, K)	500 mW
For T_A = +100 to +125°C (PACKAGE TYPES D, F, K)	Derate Linearly at 12 mW/°C to 200 mW
DEVICE DISSIPATION PER OUTPUT TRANSISTOR	
FOR T_A = FULL PACKAGE TEMPERATURE RANGE (All Package Types)	100 mW
OPERATING-TEMPERATURE RANGE (T_A)	
PACKAGE TYPES D, F, K, H	−55 to +125°C
PACKAGE TYPE E	−40 to +85°C
STORAGE TEMPERATURE RANGE (T_{stg})	−65 to +150°C
LEAD TEMPERATURE (DURING SOLDERING)	
At distance 1/16 ± 1/32 inch (1.59 ± 0.79 mm) from case for 10 s max	+265°C

RECOMMENDED OPERATING CONDITIONS

For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	LIMITS		UNITS
	Min.	Max.	
Supply-Voltage Range (For T_A = Full Package-Temperature Range)	3	18	V

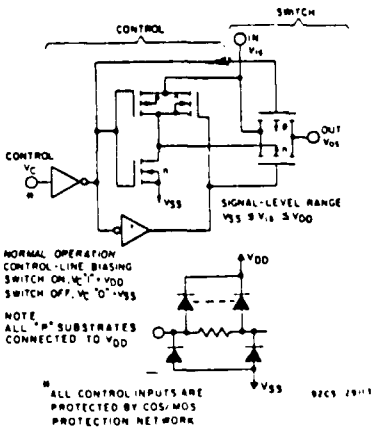
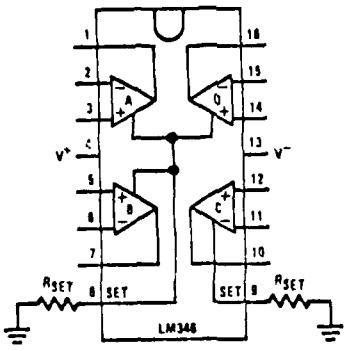


Fig.1 – Schematic diagram of 1 of 4 identical switches and its associated control circuitry.

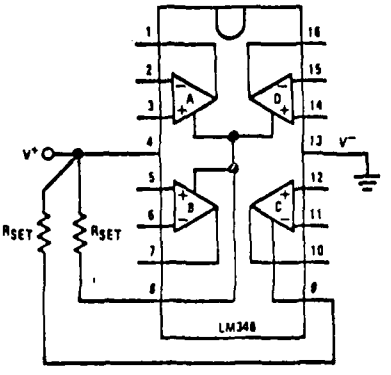
Typical Applications

Dual Supply or Negative Supply Biasing



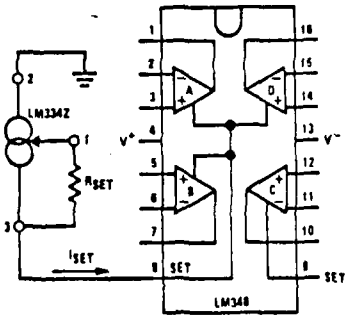
$$I_{SET} \approx \frac{|V^-| - 0.6V}{R_{SET}}$$

Single (Positive) Supply Biasing



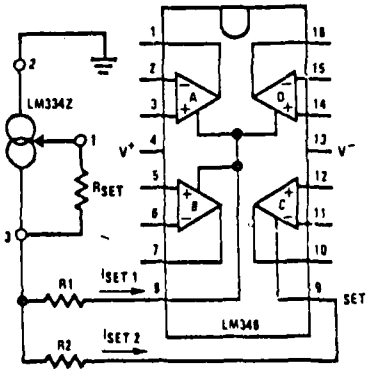
$$I_{SET} \approx \frac{V^+ - 0.6V}{R_{SET}}$$

Current Source Biasing with Temperature Compensation



$$I_{SET} = \frac{67.7\ mV}{R_{SET}}$$

Biasing all 4 Amplifiers with Single Current Source



$$\frac{I_{SET1}}{I_{SET2}} = \frac{R2}{R1},\ I_{SET1} + I_{SET2} = \frac{67.7\ mV}{R_{SET}}$$

- The LM334 provides an I_{SET} directly proportional to absolute temperature. This cancels the slight GBW product temperature coefficient of the LM346.
- For $I_{SET1} = I_{SET2}$ resistors R1 and R2 are not required if a slight error between the 2 set currents can be tolerated. If not, then use R1 = R2 to create a 100 mV drop across these resistors

Application Hints

Avoid reversing the power supply polarity, the device will fail.

Common-Mode Input Voltage: The negative common-mode voltage limit is one diode drop above the negative supply voltage. Exceeding this limit on either input will result in an output phase reversal. The positive common-mode limit is typically 1V below the positive supply voltage. No output phase reversal will occur if this limit is exceeded by either input.

Output Voltage Swing vs I_{SET}: For a desired output voltage swing the value of the minimum load depends on the positive and negative output curent capability of the op amp. The maximum available positive output current, (I_{CL+}), of the device increases with I_{SET} whereas the negative output current (I_{CL-}) is independent of I_{SET}. *Figure 1* illustrates the above.

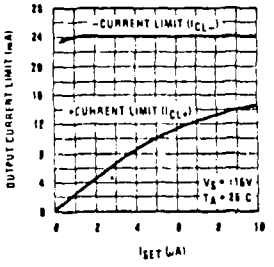


FIGURE 1. Output Current Limit vs I_{SET}

Input Capacitance: The input capacitance, C_{IN}, of the LM146 is approximately 2 pF; any stray capacitance, C_S, (due to external circuit circuit layout) will add to C_{IN}. When resistive or active feedback is applied, an additional pole is added to the open loop frequency response of the device. For instance with resistive feedback *(Figure 2)*, this pole occurs at $1/2\pi$ ($R1 \| R2$) ($C_{IN} + C_S$). Make sure that this pole occurs at least 2 octaves beyond the expected −3 dB frequency corner of the closed loop gain of the amplifier; if not, place a lead capacitor in the feedback such that the time constant of this capacitor and the resistance it parallels is equal to the $R_1(C_S + C_{IN})$, where R_1 is the input resistance of the circuit

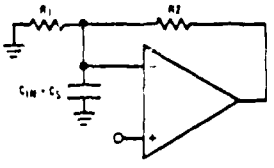


FIGURE 2

Temperature Effect on the GBW: The GBW (gain bandwidth product) of the LM146 is directly proportional to I_{SET} and inversely proportional to the absolute temperature. When using resistors to set the bias current I_{SET} of the device, the GBW product will decrease with increasing temperature. Compensation can be provided by creating an I_{SET} current directly proportional to temperature (see typical applications).

Isolation Between Amplifiers: The LM146 die is isothermally layed out such that crosstalk between *all 4* amplifiers is in excess of −105 dB (DC). Optimum isolation (better than −110 dB) occurs between amplifiers A and D, B and C; that is, if amplifier A dissipates power on its output stage, amplifier D is the one which will be affected the least, and vice versa. Same argument holds for amplifiers B and C.

LM146 Typical Performance Summary: The LM146 typical behavior is shown in *Figure 3*. The device is fully predictable. As the set current, I_{SET}, increases, the speed, the bias current, and the supply current increase while the noise power decreases proportionally and the V_{OS} remains constant. The usable GBW range of the op amp is 10 kHz to 3.5–4 MHz.

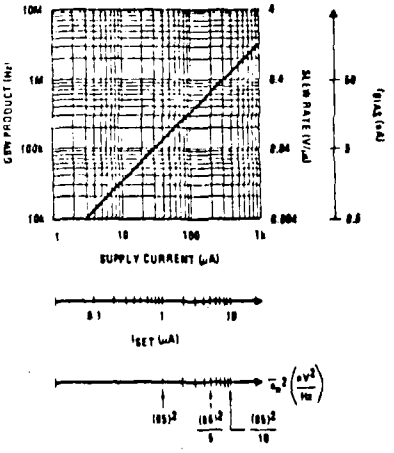


FIGURE 3. LM146 Typical Characteristics

Low Power Supply Operation: The quad op amp operates down to ±1.3V supply. Also, since the internal circuitry is biased through programmable current sources, no degradation of the device speed will occur.

Speed vs Power Consumption: LM146 vs LM4250 (single programmable). Through *Figure 4*, we observe that the LM146's power consumption has been optimized for GBW products above 200 kHz, whereas the LM4250 will reach a GBW of no more than 300 kHz, for GBW products below 200 kHz, the LM4250 will consume less.

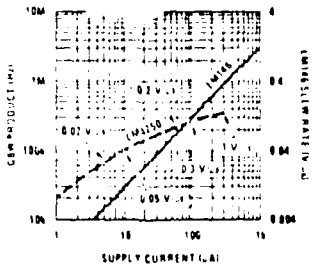
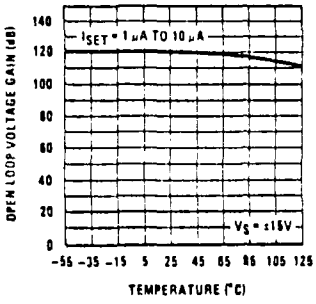


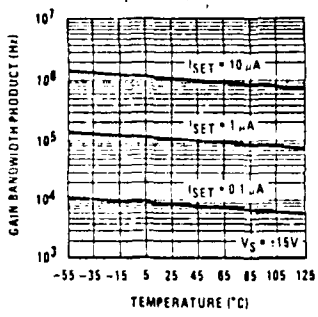
FIGURE 4 LM146 vs LM4250

Typical Performance Characteristics (Continued)

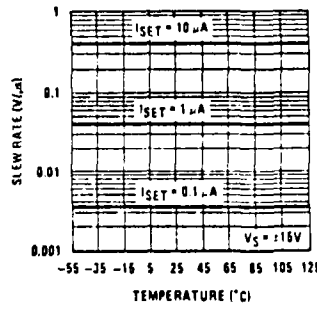
Open Loop Voltage Gain vs Temperature



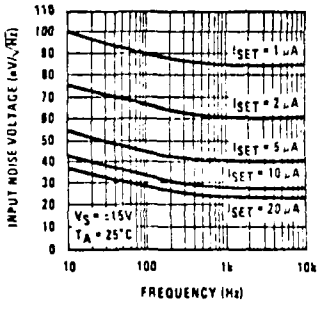
Gain Bandwidth Product vs Temperature



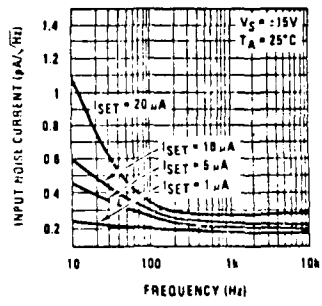
Slew Rate vs Temperature



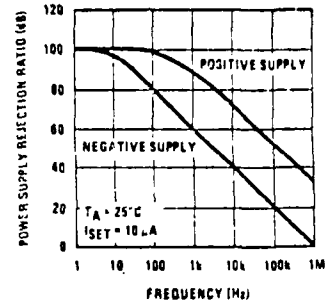
Input Noise Voltage vs Frequency



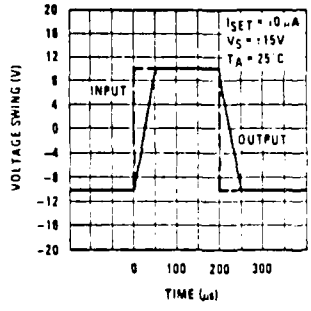
Input Noise Current vs Frequency



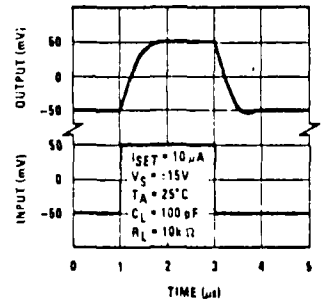
Power Supply Rejection Ratio vs Frequency



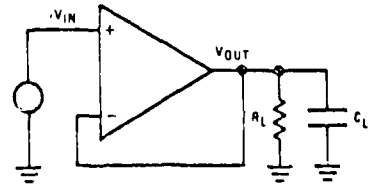
Voltage Follower Pulse Response



Voltage Follower Transient Response

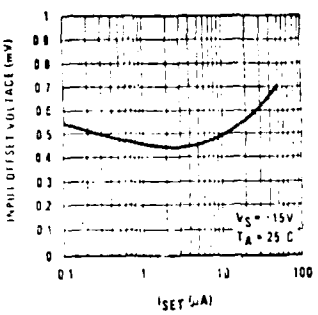


Transient Response Test Circuit

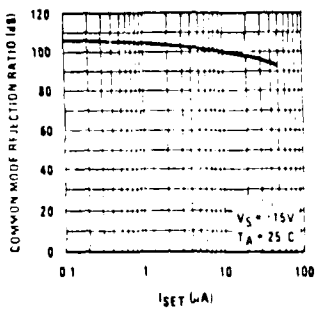


Typical Performance Characteristics (Continued)

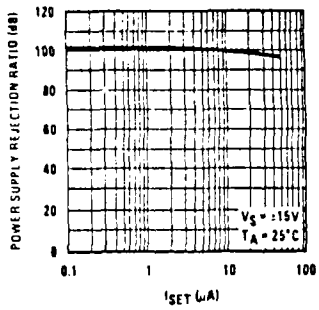
Input Offset Voltage vs I_{SET}



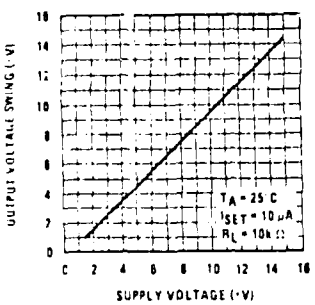
Common-Mode Rejection Ratio vs I_{SET}



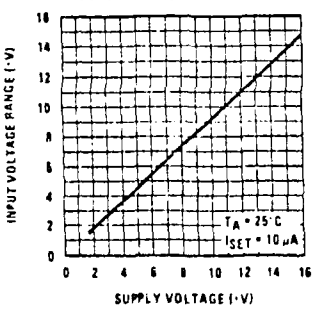
Power Supply Rejection Ratio vs I_{SET}



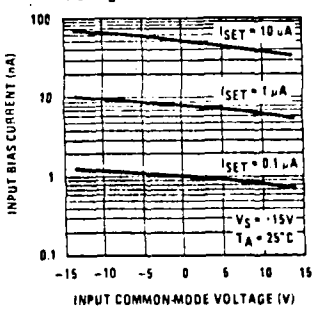
Output Voltage Swing vs Supply Voltage



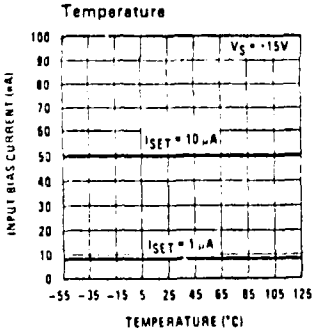
Input Voltage Range vs Supply Voltage



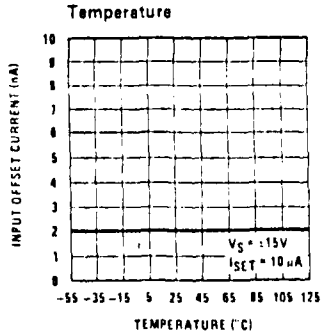
Input Bias Current vs Input Common-Mode Voltage



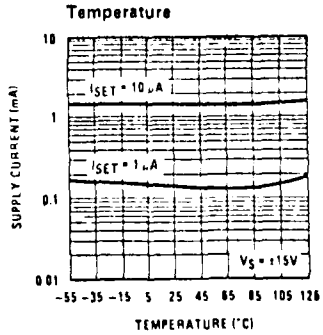
Input Bias Current vs Temperature



Input Offset Current vs Temperature



Supply Current vs Temperature



TYPES 2N2217 THRU 2N2222, 2N2218A, 2N2219A, 2N2221A, 2N2222A
N-P-N SILICON TRANSISTORS

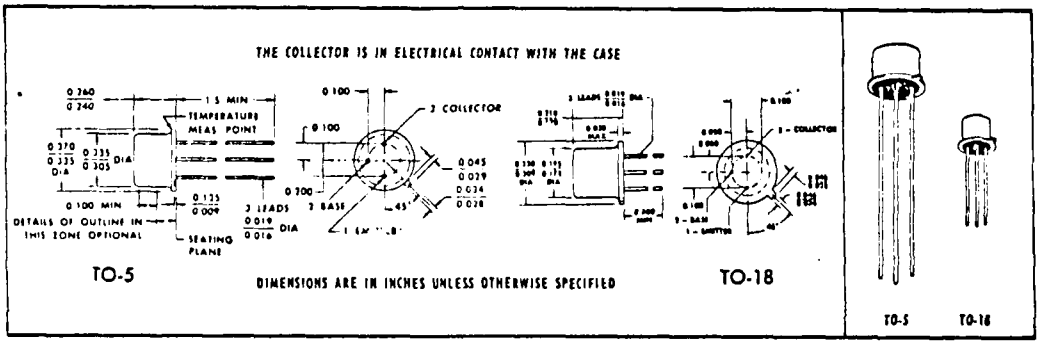
BULLETIN NO. DL S 7311916, MARCH 1973

DESIGNED FOR HIGH-SPEED, MEDIUM-POWER SWITCHING
AND GENERAL PURPOSE AMPLIFIER APPLICATIONS

- h_{FE} . . . Guaranteed from 100 μA to 500 mA
- High f_T at 20 V, 20 mA . . . 300 MHz (2N2219A, 2N2222A)
  250 MHz (all others)
- 2N2218, 2N2221 for Complementary Use with 2N2904, 2N2906
- 2N2219, 2N2222 for Complementary Use with 2N2905, 2N2906

*mechanical data

Device types 2N2217, 2N2218, 2N2218A, 2N2219, and 2N2219A are in JEDEC TO-5 packages.
Device types 2N2220, 2N2221, 2N2221A, 2N2222, and 2N2222A are in JEDEC TO-18 packages.



*absolute maximum ratings at 25°C free-air temperature (unless otherwise noted)

	2N2217 2N2218 2N2219	2N2218A 2N2219A	2N2220 2N2221 2N2222	2N2221A 2N2222A	UNIT
Collector-Base Voltage	60	75	60	75	V
Collector-Emitter Voltage (See Note 1)	30	40	30	40	V
Emitter-Base Voltage	5	6	5	6	V
Continuous Collector Current	0.8	0.8	0.8	0.8	A
Continuous Device Dissipation at (or below) 25°C Free-Air Temperature (See Notes 2 and 3)	0.8	0.8	0.5	0.5	W
Continuous Device Dissipation at (or below) 25°C Case Temperature (See Notes 4 and 5)	3	3	1.8	1.8	W
Operating Collector Junction Temperature Range	−65 to 175				°C
Storage Temperature Range	−65 to 200				°C
Lead Temperature 1/16 Inch from Case for 10 Seconds	230				°C

NOTES 1. These values apply between 0 and 500 mA collector current when the base-emitter diode is open-circuited.
2. Derate 2N2217, 2N2218, 2N2218A, 2N2219, and 2N2219A linearly to 175°C free-air temperature at the rate of 5.33 mW/°C.
3. Derate 2N2220, 2N2221, 2N2221A, 2N2222, and 2N2222A linearly to 175°C free-air temperature at the rate of 3.33 mW/°C.
4. Derate 2N2217, 2N2218, 2N2218A, 2N2219, and 2N2219A linearly to 175°C case temperature at the rate of 20.0 mW/°C.
5. Derate 2N2220, 2N2221, 2N2221A, 2N2222, and 2N2222A linearly to 175°C case temperature at the rate of 12.0 mW/°C.

*JEDEC registered data. This data sheet contains all applicable registered data in effect at the time of publication.

USES CHIP N24

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TYPES 2N2217 THRU 2N2222, 2N2218A, 2N2219A, 2N2221A, 2N2222A
N-P-N SILICON TRANSISTORS

2N2217 THRU 2N2222

*electrical characteristics at 25°C free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	TO-5→ / TO-18→	2N2217 / 2N2220		2N2218 / 2N2221		2N2219 / 2N2222		UNIT
				MIN	MAX	MIN	MAX	MIN	MAX	
$V_{(BR)CBO}$	Collector-Base Breakdown Voltage	I_C = 10 μA, I_E = 0		60		60		60		V
$V_{(BR)CEO}$	Collector-Emitter Breakdown Voltage	I_C = 10 mA, I_B = 0,	See Note 6	30		30		30		V
$V_{(BR)EBO}$	Emitter-Base Breakdown Voltage	I_E = 10 μA, I_C = 0		5		5		5		V
I_{CBO}	Collector Cutoff Current	V_{CB} = 50 V, I_E = 0			10		10		10	nA
		V_{CB} = 50 V, I_E = 0,	T_A = 150°C		10		10		10	μA
I_{EBO}	Emitter Cutoff Current	V_{EB} = 3 V, I_C = 0			10		10		10	nA
h_{FE}	Static Forward Current Transfer Ratio	V_{CE} = 10 V, I_C = 100 μA				20		35		
		V_{CE} = 10 V, I_C = 1 mA		12		25		50		
		V_{CE} = 10 V, I_C = 10 mA	See Note 6	17		35		75		
		V_{CE} = 10 V, I_C = 150 mA	See Note 6	20	60	40	120	100	300	
		V_{CE} = 10 V, I_C = 500 mA	See Note 6			20		30		
		V_{CE} = 1 V, I_C = 150 mA	See Note 6	10		20		50		
V_{BE}	Base-Emitter Voltage	I_B = 15 mA, I_C = 150 mA	See Note 6		1.3		1.3		1.3	V
		I_B = 50 mA, I_C = 500 mA	See Note 6				2.6		2.6	
$V_{CE(sat)}$	Collector-Emitter Saturation Voltage	I_B = 15 mA, I_C = 150 mA	See Note 6		0.4		0.4		0.4	V
		I_B = 50 mA, I_C = 500 mA	See Note 6				1.6		1.6	
$\lvert h_{fe} \rvert$	Small-Signal Common-Emitter Forward Current Transfer Ratio	V_{CE} = 20 V, I_C = 20 mA,	f = 100 MHz	2.5		2.5		2.5		
f_T	Transition Frequency	V_{CE} = 20 V, I_C = 20 mA,	See Note 7	250		250		250		MHz
C_{obo}	Common-Base Open-Circuit Output Capacitance	V_{CB} = 10 V, I_E = 0,	f = 1 MHz		8		8		8	pF
$h_{ie(real)}$	Real Part of Small-Signal Common-Emitter Input Impedance	V_{CE} = 20 V, I_C = 20 mA,	f = 300 MHz	60		60		60		Ω

NOTES: 6. These parameters must be measured using pulse techniques. t_w = 300 μs, duty cycle ≤ 2%.
7. To obtain f_T, the $|h_{fe}|$ response with frequency is extrapolated at the rate of −6 dB per octave from f = 100 MHz to the frequency at which $|h_{fe}|$ = 1.

switching characteristics at 25°C free-air temperature

PARAMETER		TEST CONDITIONS†		TYP	UNIT
t_d	Delay Time	V_{CC} = 30 V,	I_C = 150 mA, $I_{B(1)}$ = 15 mA,	5	ns
t_r	Rise Time	$V_{BE(off)}$ = −0.5 V,	See Figure 1	15	ns
t_s	Storage Time	V_{CC} = 30 V,	I_C = 150 mA, $I_{B(1)}$ = 15 mA,	190	ns
t_f	Fall Time	$I_{B(2)}$ = −15 mA,	See Figure 2	23	ns

†Voltage and current values shown are nominal; exact values vary slightly with transistor parameters.

*JEDEC registered data

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2N2218A, 2N2219A, 2N2221A, 2N2222A

*electrical characteristics at 25°C free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	TO-5→ / TO-18→	2N2218A / 2N2221A MIN	2N2218A / 2N2221A MAX	2N2219A / 2N2222A MIN	2N2219A / 2N2222A MAX	UNIT
$V_{(BR)CBO}$	Collector-Base Breakdown Voltage	I_C = 10 μA, I_E = 0		75		75		V
$V_{(BR)CEO}$	Collector-Emitter Breakdown Voltage	I_C = 10 mA, I_B = 0,	See Note 6	40		40		V
$V_{(BR)EBO}$	Emitter-Base Breakdown Voltage	I_E = 10 μA, I_C = 0		6		6		V
I_{CBO}	Collector Cutoff Current	V_{CB} = 60 V, I_E = 0			10		10	nA
		V_{CB} = 60 V, I_E = 0,	T_A = 150°C		10		10	μA
I_{CEV}	Collector Cutoff Current	V_{CE} = 60 V, V_{BE} = −3 V			10		10	nA
I_{BEV}	Base Cutoff Current	V_{CE} = 60 V, V_{BE} = −3 V			−20		−20	nA
I_{EBO}	Emitter Cutoff Current	V_{EB} = 3 V, I_C = 0			10		10	nA
h_{FE}	Static Forward Current Transfer Ratio	V_{CE} = 10 V, I_C = 100 μA		20		35		
		V_{CE} = 10 V, I_C = 1 mA		25		50		
		V_{CE} = 10 V, I_C = 10 mA		35		75		
		V_{CE} = 10 V, I_C = 150 mA		40	120	100	300	
		V_{CE} = 10 V, I_C = 500 mA	See Note 6	25		40		
		V_{CE} = 1 V, I_C = 150 mA		20		50		
		V_{CE} = 10 V, I_C = 10 mA, T_A = −55°C		15		35		
V_{BE}	Base-Emitter Voltage	I_B = 15 mA, I_C = 150 mA	See Note 6	0.6	1.2	0.6	1.2	V
		I_B = 50 mA, I_C = 500 mA			2		2	
$V_{CE(sat)}$	Collector-Emitter Saturation Voltage	I_B = 15 mA, I_C = 150 mA	See Note 6		0.3		0.3	V
		I_B = 50 mA, I_C = 500 mA			1		1	
h_{ie}	Small-Signal Common-Emitter Input Impedance	V_{CE} = 10 V, I_C = 1 mA	f = 1 kHz	1	3.5	2	8	kΩ
		V_{CE} = 10 V, I_C = 10 mA		0.2	1	0.25	1.25	
h_{fe}	Small-Signal Forward Current Transfer Ratio	V_{CE} = 10 V, I_C = 1 mA		30	150	50	300	
		V_{CE} = 10 V, I_C = 10 mA		50	300	75	375	
h_{re}	Small-Signal Common-Emitter Reverse Voltage Transfer Ratio	V_{CE} = 10 V, I_C = 1 mA			5×10^{-4}		8×10^{-4}	
		V_{CE} = 10 V, I_C = 10 mA			2.5×10^{-4}		4×10^{-4}	
h_{oe}	Small-Signal Common-Emitter Output Admittance	V_{CE} = 10 V, I_C = 1 mA		3	15	5	35	μmho
		V_{CE} = 10 V, I_C = 10 mA		10	100	25	200	
$\lvert h_{fe} \rvert$	Small-Signal Common-Emitter Forward Current Transfer Ratio	V_{CE} = 20 V, I_C = 20 mA,	f = 100 MHz	2.5		3		
f_T	Transition Frequency	V_{CE} = 20 V, I_C = 20 mA,	See Note 7	250		300		MHz
C_{obo}	Common-Base Open-Circuit Output Capacitance	V_{CB} = 10 V, I_E = 0,	f = 100 kHz		8		8	pF
C_{ibo}	Common-Base Open-Circuit Input Capacitance	V_{EB} = 0.5 V, I_C = 0,	f = 100 kHz		25		25	pF
$h_{ie(real)}$	Real Part of Small-Signal Common-Emitter Input Impedance	V_{CE} = 20 V, I_C = 20 mA,	f = 300 MHz		60		60	Ω
$r_b'C_c$	Collector-Base Time Constant	V_{CE} = 20 V, I_C = 20 mA,	f = 31.8 MHz		150		150	ps

NOTES: 6. These parameters must be measured using pulse techniques. t_w = 300 μs, duty cycle ≤ 2%.
7. To obtain f_T, the $|h_{fe}|$ response with frequency is extrapolated at the rate of −6 dB per octave from f = 100 MHz to the frequency at which $|h_{fe}|$ = 1.

*JEDEC registered data

*operating characteristics at 25°C free-air temperature

PARAMETER		TEST CONDITIONS	TO-5→ / TO-18→	2N2218A / 2N2221A	2N2219A / 2N2222A	UNIT
				MAX	MAX	
F	Spot Noise Figure	V_{CE} = 10 V, I_C = 100 μA, R_G = 1 kΩ, f = 1 kHz			4	dB

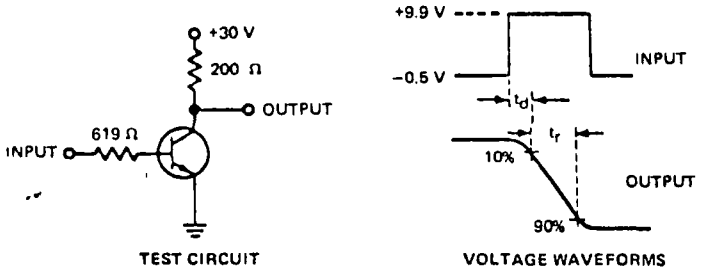
*switching characteristics at 25°C free-air temperature

PARAMETER		TEST CONDITIONS†	TO-5→ / TO-18→	2N2218A / 2N2221A	2N2219A / 2N2222A	UNIT
				MAX	MAX	
t_d	Delay Time	V_{CC} = 30 V, I_C = 150 mA, $I_{B(1)}$ = 15 mA, $V_{BE(off)}$ = −0.5 V, See Figure 1		10	10	ns
t_r	Rise Time			25	25	ns
τ_A	Active Region Time Constant‡			2.5	2.5	ns
t_s	Storage Time	V_{CC} = 30 V, I_C = 150 mA, $I_{B(1)}$ = 15 mA, $I_{B(2)}$ = −15 mA, See Figure 2		225	225	ns
t_f	Fall Time			60	60	ns

†*Voltage and current values shown are nominal; exact values vary slightly with transistor parameters.*

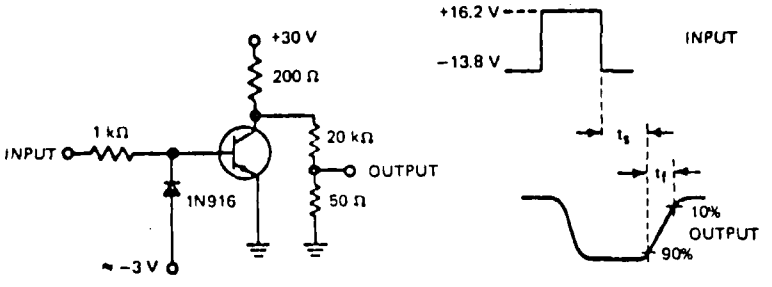
‡Under the given conditions τ_A is equal to $\frac{t_r}{10}$.

*PARAMETER MEASUREMENT INFORMATION



TEST CIRCUIT VOLTAGE WAVEFORMS

FIGURE 1–DELAY AND RISE TIMES



TEST CIRCUIT VOLTAGE WAVEFORMS

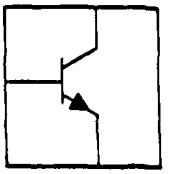
FIGURE 2–STORAGE AND FALL TIMES

NOTES: a. The input waveforms have the following characteristics: For Figure 1, $t_r \leq 2$ ns, $t_w \leq 200$ ns, duty cycle ≤ 2%; for Figure 2, $t_f \leq 5$ ns, $t_w \approx 100$ μs, duty cycle ≤ 17%.
b. All waveforms are monitored on an oscilloscope with the following characteristics: $t_r \leq 5$ ns, $R_{in} \geq 100$ kΩ, $C_{in} \leq 12$ pF.

*JEDEC registered data

CHIP TYPE N24
N-P-N SILICON TRANSISTORS

- N24 is a 19 X 19-mil, epitaxial, planar, direct-contact chip
- Available in TO-5, TO-18, TO-39, a short-can version of TO-78, plastic dual-in-line quad, and *Silect*† packages
- For use in general purpose amplifier and medium-current switching circuits



electrical and operating characteristics at 25°C free-air temperature

PARAMETER		CONDITIONS			OBSERVED VALUES LOW	TYP	HIGH	UNIT
$V_{(BR)CBO}$	Collector-Base Breakdown Voltage	I_C = 100 μA,	I_E = 0		80♦	100		V
$V_{(BR)CEO}$	Collector-Emitter Breakdown Voltage	I_C = 10 mA,	I_B = 0,	See Note 1	35♦	45		V
$V_{(BR)EBO}$	Emitter-Base Breakdown Voltage	I_E = 100 μA,	I_C = 0		6♦	6.5		V
I_{CBO}	Collector Cutoff Current	V_{CB} = 50 V,	I_E = 0			<1	100	nA
I_{EBO}	Emitter Cutoff Current	V_{EB} = 4 V,	I_C = 0			<1	100	nA
h_{FE}	Static Forward Current Transfer Ratio	V_{CE} = 10 V,	I_C = 1 mA		20	70		
		V_{CE} = 10 V,	I_C = 10 mA	See Note 1	50	100		
		V_{CE} = 10 V,	I_C = 150 mA		50	120	600	
		V_{CE} = 10 V,	I_C = 500 mA		20	95		
V_{BE}	Base-Emitter Voltage	I_B = 15 mA,	I_C = 150 mA	See Note 1		0.95	1	V
		I_B = 50 mA,	I_C = 500 mA			1.15		
$V_{CE(sat)}$	Collector-Emitter Saturation Voltage	I_B = 15 mA,	I_C = 150 mA	See Note 1		0.15	0.3	V
		I_B = 50 mA,	I_C = 500 mA			0.4		
h_{ie}	Small-Signal Common-Emitter Input Impedance	V_{CE} = 10 V,	I_C = 1 mA,	f = 1 kHz	0.5	2		kΩ
h_{fe}	Small-Signal Common-Emitter Forward Current Transfer Ratio				20	75		
h_{re}	Small-Signal Common-Emitter Reverse Voltage Transfer Ratio					0.8 x 10^{-4}	6 x 10^{-4}	
h_{oe}	Small-Signal Common-Emitter Output Admittance					6	20	μmho
f_T	Transition Frequency	V_{CE} = 10 V,	I_C = 50 mA,	f = 100 MHz	100	400		MHz
C_{obo}	Common-Base Open-Circuit Output Capacitance	V_{CB} = 10 V,	I_E = 0	f = 1 MHz, See Notes 2 and 3		4.5	12	pF
C_{ibo}	Common-Base Open-Circuit Input Capacitance	V_{EB} = 0.5 V,	I_C = 0			20	30	pF
C_{cb}	Collector-Base Capacitance	V_{CB} = 10 V	I_E = 0			4.0		pF
t_d	Delay Time	V_{CC} = 30 V,	I_C = 150 mA,	2N2218A Data Sheet Circuit		5		ns
t_r	Rise Time	$I_{B(1)}$ = 15 mA,	$V_{BE(off)}$ = −0.5 V			15		
t_s	Storage Time	V_{CC} = 30 V,	I_C = 150 mA,			190		
t_f	Fall Time	$I_{B(1)}$ = 15 mA,	$I_{B(2)}$ = −15 mA			23		
t_d	Delay Time	V_{CC} = 30 V,	I_C = 150 mA,			6		ns
t_r	Rise Time	$V_{BE(off)}$ = −4.1 V,	See Figure 1			15		
t_s	Storage Time	V_{CC} = 30 V,	I_C = 150 mA,	$I_{B(1)}$ = 15 mA,		190		
t_f	Fall Time	$I_{B(2)}$ = −15 mA				23		

†Trademark of Texas Instruments

♦These values do not modify guaranteed limits for specific devices and do not justify operation in excess of absolute maximum ratings.

NOTES: 1. These parameters were measured using pulse techniques t_w = 300 μs, duty cycle ≤ 2%.

2. Capacitance measurements were made using chips mounted in TO-5 packages.

3. C_{cb} measurement employs a three-terminal capacitance bridge incorporating a guard circuit. The emitter is connected to the guard terminal of the bridge. C_{obo} and C_{ibo} measurements are made with the third terminal floating.

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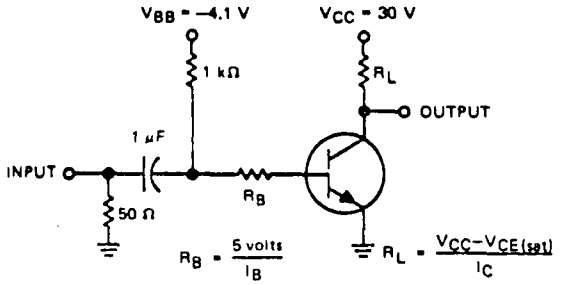
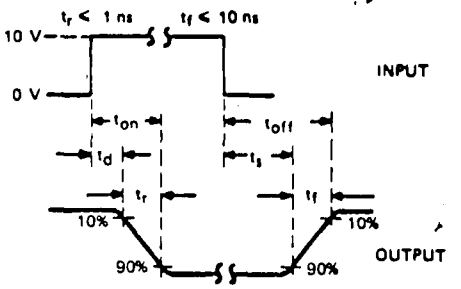
PARAMETER MEASUREMENT INFORMATION



TEST CIRCUIT



(See Notes a and b)
VOLTAGE WAVEFORMS

NOTES: a. The input waveforms are supplied by a generator with the following characteristics: Z_{out} = 50 Ω, for measuring t_d and t_r, t_w = 200 ns, duty cycle ≤ 2%; for measuring t_s and t_f, t_w = 10 μs, duty cycle ≤ 2%.
b. Waveforms are monitored on an oscilloscope with the following characteristics: t_r = 1 ns, R_{in} ≥ 100 kΩ, C_{in} ≤ 7 pF.

FIGURE 1–SWITCHING TIMES

TYPICAL CHARACTERISTICS

I_{CBO} vs T_A

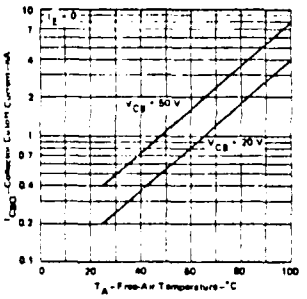


FIGURE 2

Normalized h_{FE} vs I_C

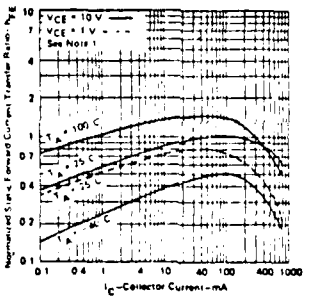


FIGURE 3

V_{BE} vs I_C

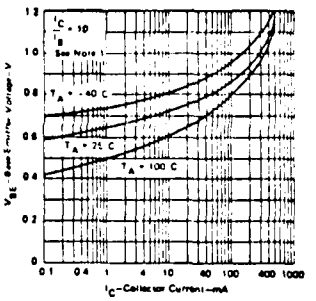


FIGURE 4

V_{BE} vs I_C

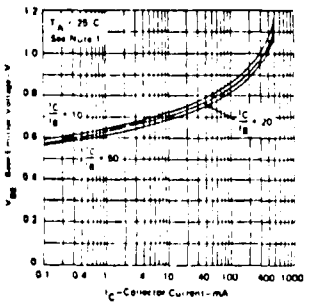


FIGURE 5

$V_{CE(sat)}$ vs I_C

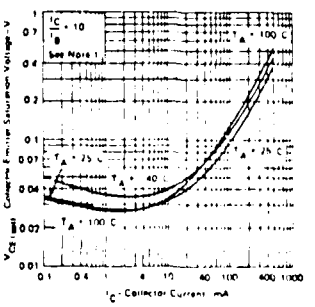


FIGURE 6

$V_{CE(sat)}$ vs I_C

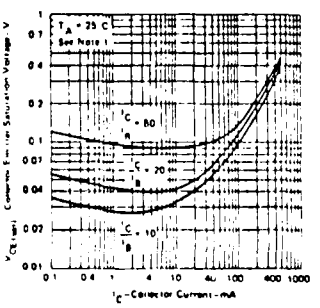


FIGURE 7

NOTE 1: These parameters were measured using pulse techniques t_w = 300 μs, duty cycle ≤ 2%.

CHIP TYPE N24
N-P-N SILICON TRANSISTORS

TYPICAL CHARACTERISTICS

Normalized h_{ie}, h_{fe}, h_{re}, h_{oe} vs I_C

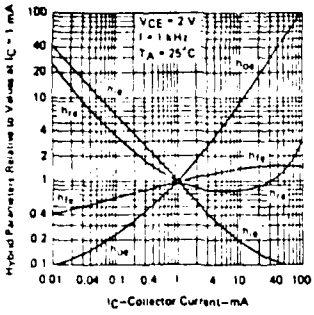


FIGURE 8

f_T vs I_C

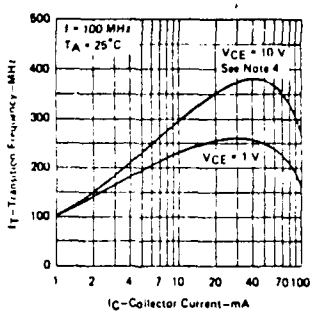


FIGURE 9

C_{obo}, C_{ibo}, C_{cb} vs V_R

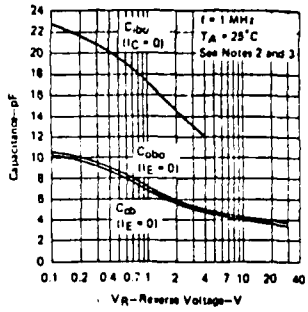


FIGURE 10

t_d vs I_C

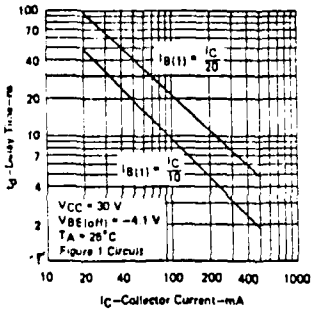


FIGURE 11

t_r vs I_C

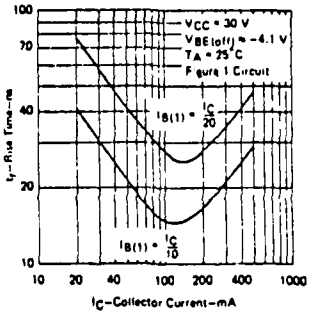


FIGURE 12

t_s vs I_C

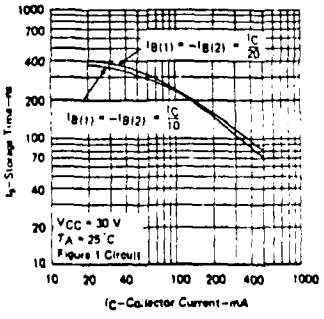


FIGURE 13

t_f vs I_C

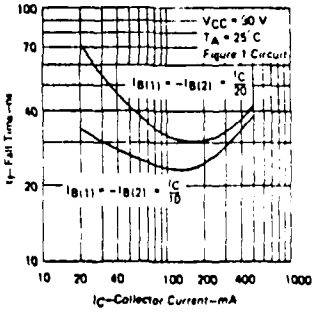


FIGURE 14

NOTES: 2. Capacitance measurements were made using chips mounted in TO-5 packages.

3. C_{cb} measurement employs a three-terminal capacitance bridge incorporating a guard circuit. The emitter is connected to the guard terminal of the bridge. C_{obo} and C_{ibo} measurements are made with the third terminal floating.

4. To avoid overheating the transistor, this parameter was measured with bias conditions applied for less than 5 seconds.

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

National Semiconductor

Industrial Blocks

LM733/LM733C Differential Video Amp

General Description

The LM733/LM733C is a two-stage, differential input, differential output, wide-band video amplifier. The use of internal series-shunt feedback gives wide bandwidth with low phase distortion and high gain stability. Emitter-follower outputs provide a high current drive, low impedance capability. It's 120 MHz bandwidth and selectable gains of 10, 100, and 400, without need for frequency compensation, make it a very useful circuit for memory element drivers, pulse amplifiers, and wide band linear gain stages.

The LM733 is specified for operation over the −55°C to +125°C military temperature range. The LM733C is specified for operation over the 0°C to +70°C temperature range.

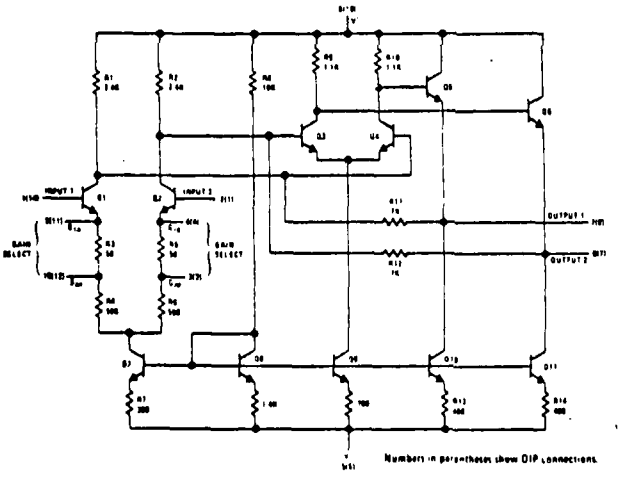
Features

- 120 MHz bandwidth
- 250 kΩ input resistance
- Selectable gains of 10, 100, 400
- No frequency compensation
- High common mode rejection ratio at high frequencies.

Applications

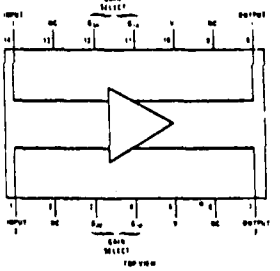
- Magnetic tape systems
- Disk file memories
- Thin and thick film memories
- Woven and plated wire memories
- Wide band video amplifiers.

Schematic and Connection Diagrams



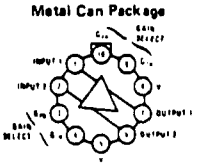
Numbers in parentheses show DIP connections.

Dual-In-Line Package



Order Number LM733CN
See NS Package N14A

Metal Can Package

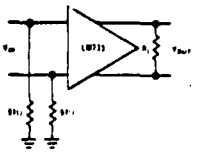


Note: Pin 5 connected to case

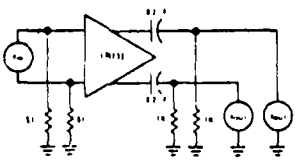
Order Number LM733H or LM733CH
See NS Package H10D

Test Circuits

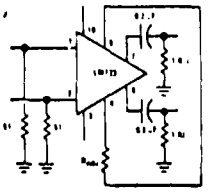
Test Circuit 1



Test Circuit 2



Voltage Gain Adjust Circuit



$V_S = 6V, T_A = 25°C$

(The numbers apply to TO 5 package)

Absolute Maximum Ratings

Differential Input Voltage	±5V
Common Mode Input Voltage	±6V
V_{CC}	±8V
Output Current	10 mA
Power Dissipation (Note 1)	500 mW
Junction Temperature	+150°C
Storage Temperature Range	-65°C to +150°C
Operating Temperature Range LM733	-55°C to +125°C
LM733C	0°C to +70°C
Lead Temperature (Soldering, 10 sec)	300°C

Electrical Characteristics (T_A = 25°C, unless otherwise specified, see test circuits, V_S = ±6.0V)

CHARACTERISTICS	TEST CIRCUIT	TEST CONDITIONS	LM733			LM733C			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
Differential Voltage Gain									
Gain 1 (Note 2)			300	400	500	250	400	600	
Gain 2 (Note 3)	1	R_L = 2 kΩ V_{OUT} = 3 V_{pp}	90	100	110	80	100	120	
Gain 3 (Note 4)			9.0	10	11	8.0	10	12	
Bandwidth									
Gain 1				40			40		MHz
Gain 2	2			90			90		MHz
Gain 3				120			120		MHz
Rise Time									
Gain 1		V_{OUT} = 1 V_{pp}		10.5			10.5		ns
Gain 2	2			4.5	10		4.5	12	ns
Gain 3				2.5			2.5		ns
Propagation Delay		V_{OUT} = 1 V_{pp}							
Gain 1				7.5			7.5		ns
Gain 2	2			6.0	10		6.0	10	ns
Gain 3				3.6			3.6		ns
Input Resistance									
Gain 1				4.0			4.0		kΩ
Gain 2			20	30		10	30		kΩ
Gain 3				250			250		kΩ
Input Capacitance		Gain 2		2.0			2.0		pF
Input Offset Current				0.4	3.0		0.4	5.0	μA
Input Bias Current				9.0	20		9.0	30	μA
Input Noise Voltage		BW = 1 kHz to 10 MHz		12			12		μVrms
Input Voltage Range	1		±1.0			±1.0			V
Common Mode Rejection Ratio									
Gain 2	1	V_{CM} = ±1V $f \leq$ 100 kHz	60	86		60	86		dB
Gain 2		V_{CM} = ±1V f = 5 MHz		60			60		dB
Supply Voltage Rejection Ratio									
Gain 2	1	ΔV_S = ±0.5V	50	70		50	70		dB
Output Offset Voltage									
Gain 1	1	R_L = ∞		0.6	1.5		0.6	1.5	V
Gain 2 and 3				0.35	1.0		0.35	1.5	V
Output Common Mode Voltage	1	R_L = ∞	2.4	2.9	3.4	2.4	2.9	3.4	V
Output Voltage Swing	1	R_L = 2k	3.0	4.0		3.0	4.0		
Output Sink Current			2.5	3.6		2.5	3.6		mA
Output Resistance				20			20		Ω
Power Supply Current	1	R_L = ∞		18	24		18	24	mA

Electrical Characteristics (Continued)

(The following specifications apply for $-55°C < T_A < 125°C$ for the LM733 and $0°C < T_A < 70°C$ for the LM733C, $V_S = \pm 6.0V$)

CHARACTERISTICS	TEST CIRCUIT	TEST CONDITIONS	LM733			LM733C			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
Differential Voltage Gain									
Gain 1			200		600	250		600	
Gain 2	1	$R_L = 2\ k\Omega$, $V_{OUT} = 3\ V_{p-p}$	80		120	80		120	
Gain 3			8.0		12.0	8.0		12.0	
Input Resistance Gain 2			8			8			kΩ
Input Offset Current					5			6	μA
Input Bias Current					40			40	μA
Input Voltage Range	1		±1			±1			V
Common Mode Rejection Ratio									
Gain 2	1	$V_{CM} = \pm 1V$, $f \leq 100\ kHz$	50			50			dB
Supply Voltage Rejection Ratio									
Gain 2	1	$\Delta V_S = \pm 0.5V$	50			50			dB
Output Offset Voltage									
Gain 1	1	$R_L = \infty$			1.6			1.6	V
Gain 2 and 3					1.2			1.5	V
Output Voltage Swing	1	$R_L = 2k$	2.5			2.8			V_{p-p}
Output Sink Current			2.2			2.6			mA
Power Supply Current	1	$R_L = \infty$			27			27	mA

Note 1: The maximum junction temperature of the LM733 is 150°C, while that of the LM733C is 100°C. For operation at elevated temperatures devices in the TO-100 package must be derated based on a thermal resistance of 150°C/W junction to ambient or 45°C/W junction to case. Thermal resistance of the dual-in-line package is 100°C/W.

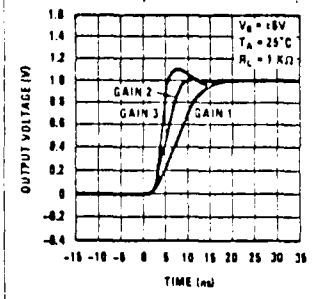
Note 2: Pins G1A and G1B connected together.

Note 3: Pins G2A and G2B connected together.

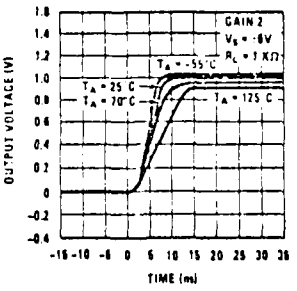
Note 4: Gain select pins open.

Typical Performance Characteristics

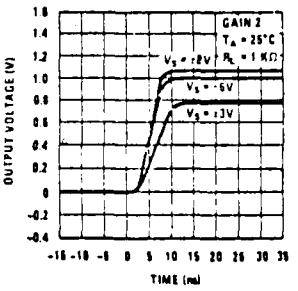
Pulse Response



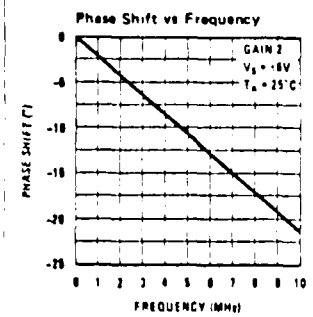
Pulse Response vs Temperature



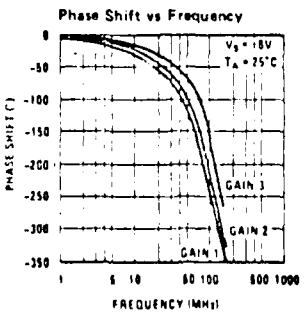
Pulse Response vs Supply Voltage



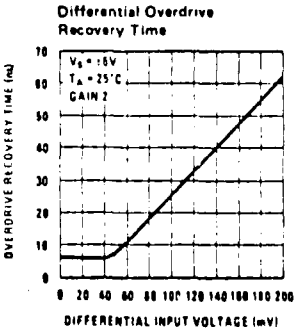
Phase Shift vs Frequency



Phase Shift vs Frequency

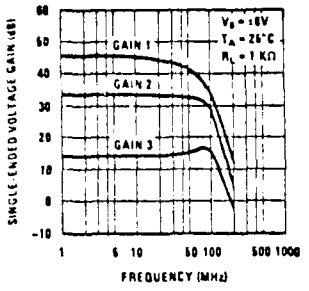


Differential Overdrive Recovery Time

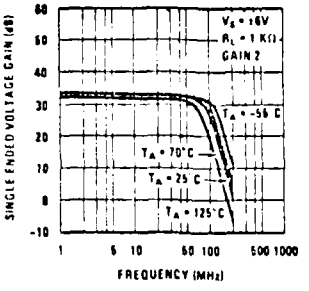


Typical Performance Characteristics (Continued)

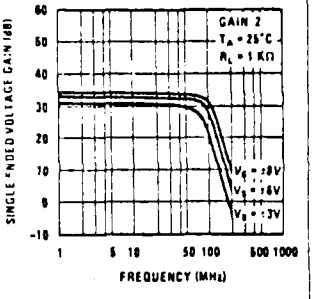
Voltage Gain vs Frequency



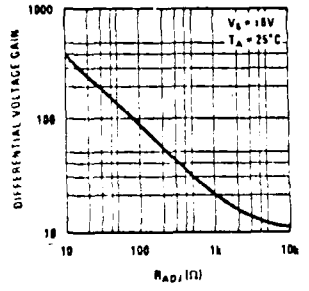
Gain vs Frequency Temperature



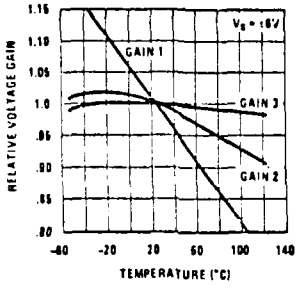
Gain vs Frequency vs Supply Voltage



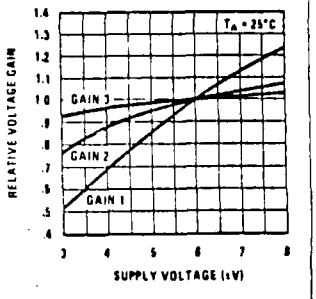
Voltage Gain vs R_{ADJ}



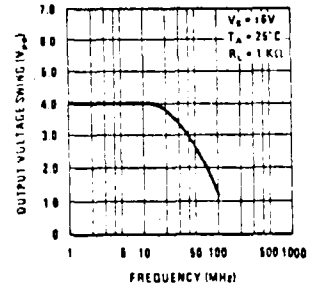
Voltage Gain vs Temperature



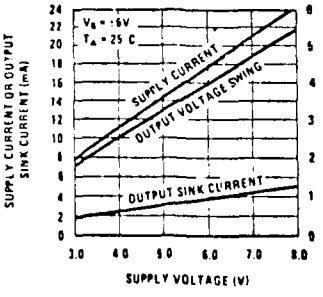
Voltage Gain vs Supply Voltage



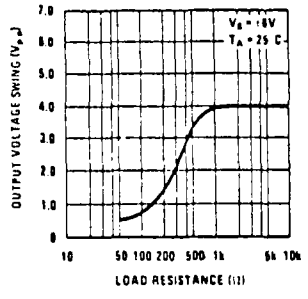
Output Voltage Swing vs Frequency



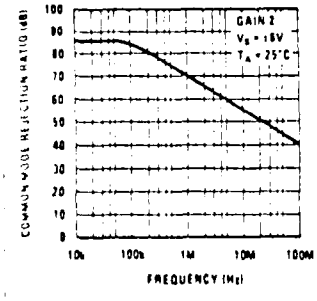
Supply Current, Output Voltage and Current Swing vs Supply Voltage



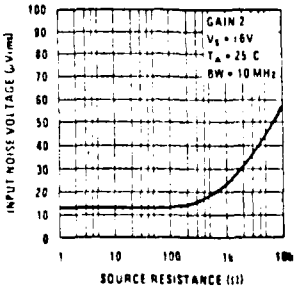
Output Voltage Swing vs Load Resistance



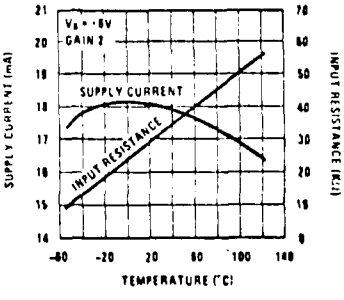
Common Mode Rejection Ratio vs Frequency



Input Noise Voltage vs Source Resistance



Supply Current and Input Resistance vs Temperature



PHASE LOCKED LOOP NE/SE564

DESCRIPTION

The NE564 is a versatile, high guaranteed frequency Phase Locked Loop designed for operation up to 50MHz. As shown in the block diagram, the NE564 consists of a VCO, limiter, phase comparator, and post detection processor.

APPLICATIONS

- High speed modems
- FSK receivers and transmitters
- Frequency synthesizers
- Signal generators
- Various satcom/TV systems

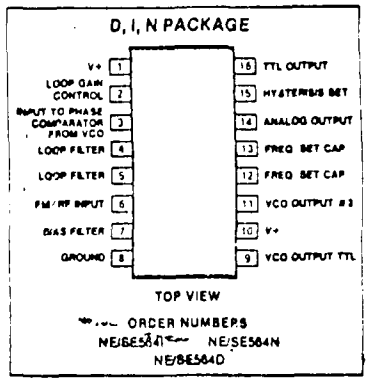
FEATURES

- Operation with single 5V supply
- TTL compatible inputs and outputs
- Guaranteed operation to 50MHz
- External loop gain control
- Reduced carrier feedthrough
- No elaborate filtering needed in FSK applications
- Can be used as a modulator
- Variable loop gain (Externally Controlled)

OUTLINE OF SETUP PROCEDURE

1. *Determine operating frequency of the* VCO – .
   If ÷ N in feedback loop, then
   $f_o = N \times f_{in}$.
2. Calculate value of the VCO frequency set capacitor:
   $$C_O \approx \frac{1}{2500\, f_o}$$
3. Set I_2 (current sinking into Pin 2) for ≅ 200μA. *After operation* is obtained, this value may be adjusted for best dynamic behavior.
4. Check VCO output frequency with digital counter at Pin 9 of device (loop open, VCO to ϕ det.). Adjust C_O trim or frequency adj. Pin 4-5 for exact center frequency if needed.
5. Close loop and inject input signal to Pin 6. Monitor Pin 3 and 6 with two channel scope. Lock should occur with $\Delta\phi_{3\text{-}6}$ equal to 90° (phase error).
6. If pulsed burst or ramp frequency is used for input signal, special loop filter design may be required in place of simple single capacitor filter on Pin 4 and 5. (See PLL application section in Analog Manual.)
7. The input signal to Pin 6 and the VCO feedback signal to Pin 3 must have a duty cycle of 50% for proper operation of the phase detector. Due to the nature of a balanced mixer if signals are not 50% in duty cycle, D.C. offsets will occur in the loop which tend to create an artificial or biased VCO offset.
8. For multiplier circuits where phase jitter is a problem, loop filter capacitors may be increased to a value of 10-50μF on Pin 4, 5. Also careful supply decoupling may be necessary. This includes the counter chain V_{CC} lines.

PIN CONFIGURATION

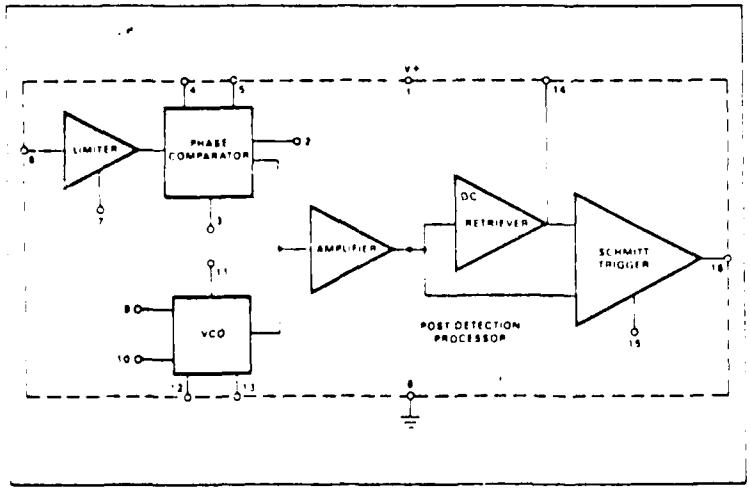


ABSOLUTE MAXIMUM RATINGS

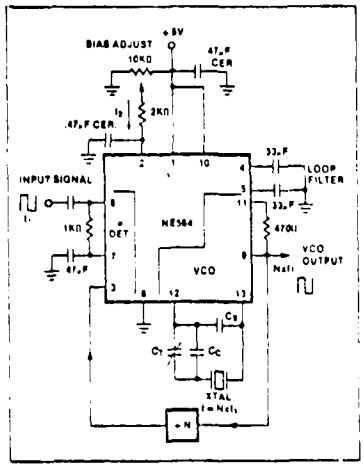
PARAMETER			RATING	UNIT
V+	Supply voltage			V
	Pin 1		14	
	Pin 10		6	
P_D	Power dissipation		600	mW
T_A	Operating temperature	NE	0 to 70	°C
	Operating temperature	SE	−65 to +125	
T_{stg}	Storage temperature		−65 to 150	°C

NOTE.
Operation above 5 volts will require heatsinking of the case.

BLOCK DIAGRAM



NE564 PHASE LOCKED FREQUENCY MULTIPLIER WITH VCXO



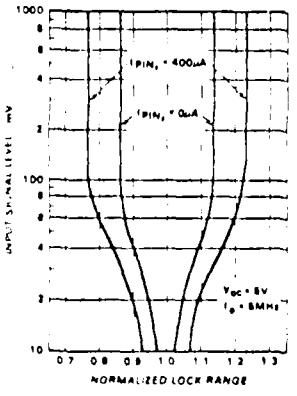
PHASE LOCKED LOOP NE/SE564

ELECTRICAL CHARACTERISTICS V_{CC} = 5V, T_A = 25°C, f_o = 5MHz, I_B = 400μA unless otherwise specified

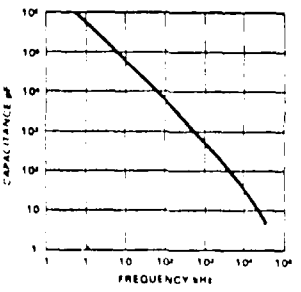
PARAMETER	TEST CONDITIONS	SE564			NE564			UNIT
		Min	Typ	Max	Min	Typ	Max	
Maximum VCO frequency	C_1 = 0	50	65		45	60		MHz
Lock range	Input ≥ 200mVrms T_A = 25°C	40	70		40	70		% of f_o
	= 125°C	20	30					
	= −55°C	50	80					
	= 0°C					70		
	= 70°C					40		
Capture range	Input ≥ 200mVrms, R_2 = 27Ω	20	30		20	30		% of f_o
VCO frequency drift with temperature	f_o = 5MHz, T_A = −55°C to 125°C		400	1000				PPM/°C
	= 0°C to 70°C					400	1250	
	f_o = 500KHz, T_A = −55°C to 125°C		250	500				
	= 0°C to 70°C					400	850	
VCO free running frequency	$f_o = \frac{1}{25R_CC_1}$, C_1 = 80pF, R_C = 100Ω "Internal"	4	5	6	3,5	5	7	MHz
VCO frequency change with supply voltage	V_{CC} = 4.5V to 5.5V		3	8		3	8	% of f_o
Demodulated output voltage	Modulation frequency: 1KHz							
	f_o = 5MHz, input deviation:							
	2%T = 25°C	16	28		16	28		mVrms
	1%T = 25°C	8	14		8	14		mVrms
	= 0°C					13		mVrms
	= −55°C	8	10					mVrms
	= 70°C					15		mVrms
	= 125°C	12	18					mVrms
Distortion	Deviation: 1% to 8%		1			1		%
Signal to noise ratio	Std. condition, 1% to 10% dev.		40			40		dB
AM rejection	Std. condition, 30% AM		35			35		dB
Demodulated Output at operating voltage	Modulation frequency: 1KHz							
	f_o = 5MHz, input deviation: 1%							
	V_{CC} = 4.5V	7	12		7	12		mVrms
	V_{CC} = 5.5V	8	14		8	14		mVrms
Supply current	V_{CC} = 5V I_1, I_{10}		45	60		45	60	mA
Output								
"1" output leakage current	V_{OUT} = 5V, Pin 16, 9		1	20		1	20	μA
"0" output voltage	I_{OUT} = 2mA, Pin 16, 9		0.3	0.6		0.3	0.6	V
	I_{OUT} = 6mA, Pin 16, 9		0.4	0.8		0.4	0.8	V

TYPICAL PERFORMANCE CHARACTERISTICS

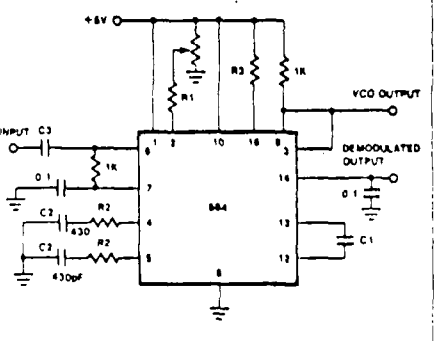
LOCK RANGE vs SIGNAL INPUT



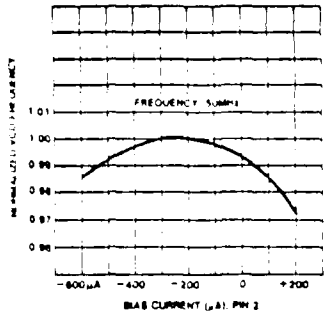
VCO CAPACITOR vs FREQUENCY



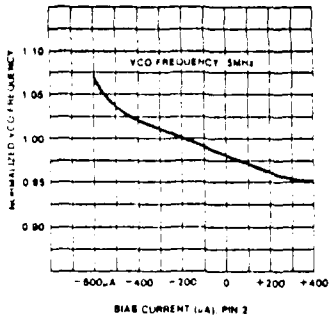
SE/NE 564 TEST CIRCUIT



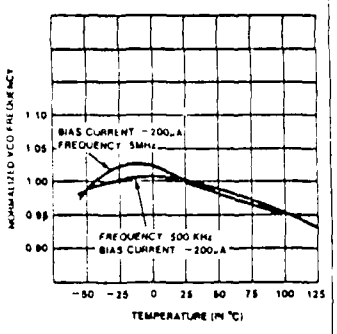
TYPICAL NORMALIZED VCO FREQUENCY AS A FUNCTION OF PIN 2 BIAS CURRENT



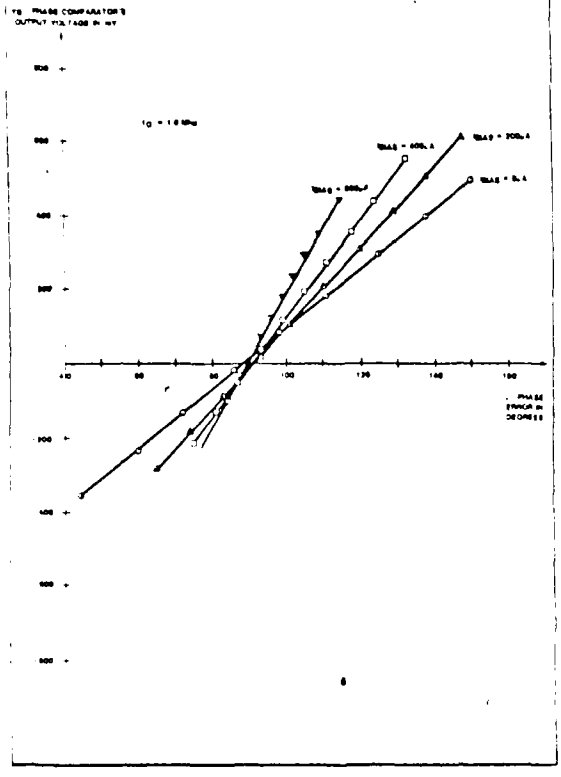
TYPICAL NORMALIZED VCO FREQUENCY AS A FUNCTION OF PIN 2 BIAS CURRENT



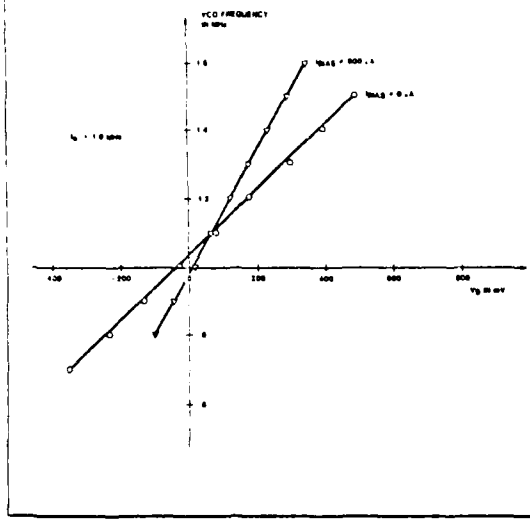
NORMALIZED VCO FREQUENCY AS A FUNCTION OF TEMPERATURE



VARIATION OF THE PHASE COMPARATOR'S OUTPUT VOLTAGE VERSUS PHASE ERROR AND BIAS CURRENT (K_D)



VCO OUTPUT FREQUENCY AS A FUNCTION OF INPUT VOLTAGE AND BIAS CURRENT (K_O)



11

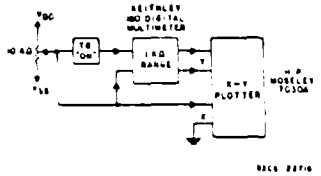


Fig. 13– Channel ON resistance measurement circuit.

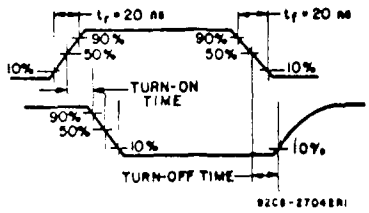


Fig. 14– Propagation delay waveform channel being turned ON (R_L = 10 K Ω, C_L = 50 pF).

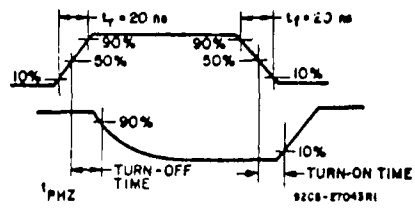


Fig. 15– Propagation delay waveform, channel being turned OFF (R_L = 300 Ω, C_L = 50 pF).

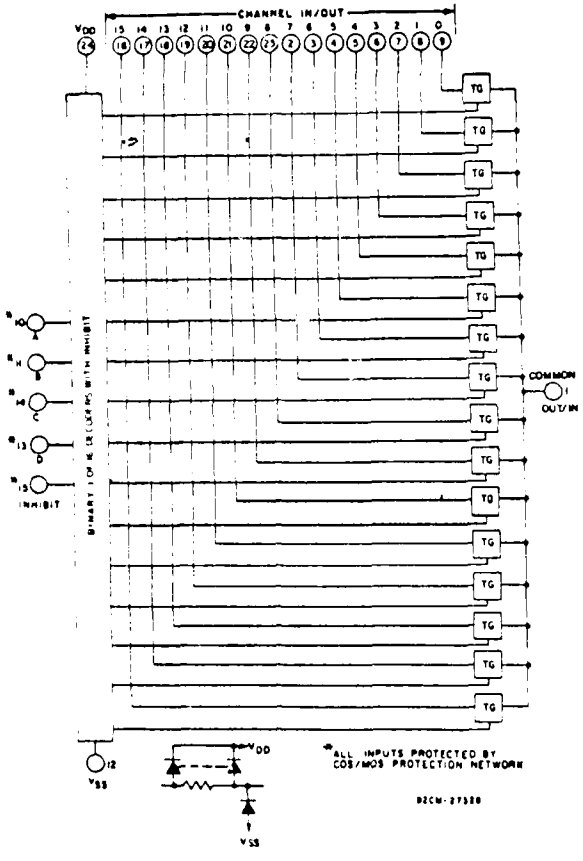


Fig. 16– CD4067 logic diagram.

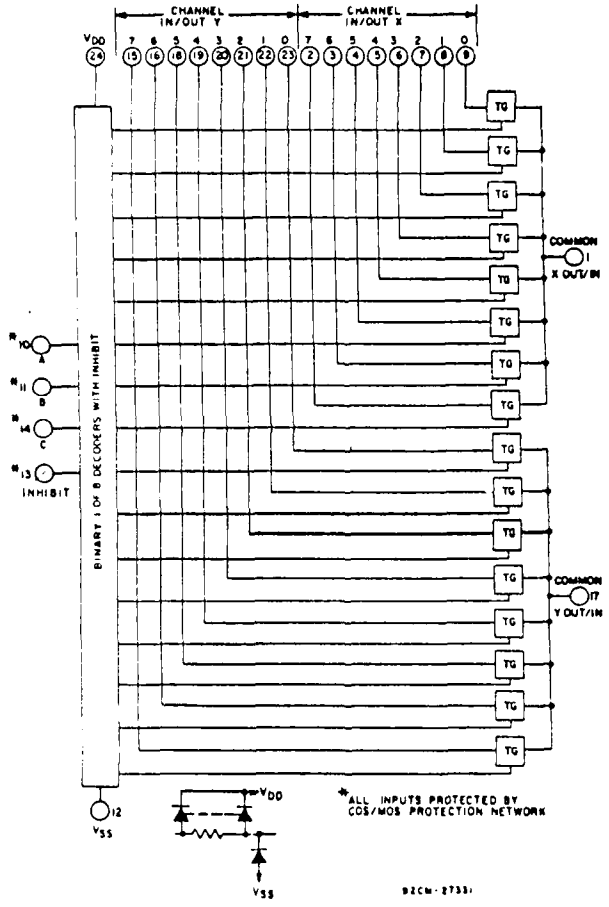


Fig. 17– CD4097 logic diagram.

ELECTRICAL CHARACTERISTICS (Cont'd)

CHARACTERISTIC	TEST CONDITIONS V_{is} (V)	V_{DD} (V)	R_L (KΩ)			TYPICAL VALUES	UNITS
Cutoff (−3-dB) Frequency Channel ON (Sine Wave Input)	5●	10	1	$20 \log \frac{V_{os}}{V_{is}} = -3$ dB	V_{os} at Common OUT/IN	CD4067	14	MHz
						CD4097	20	
					V_{os} at Any Channel		60	
Total Harmonic Distortion, THD	2●	5	10				0.3	%
	3●	10					0.2	
	5●	15					0.12	
	f_{is} = 1 kHz sine wave							
−40-dB Feedthrough Frequency (All Channels OFF	5●	10	1	$20 \log \frac{V_{os}}{V_{is}} = -40$ dB	V_{os} at Common OUT/IN	CD4067	20	MHz
						CD4097	12	
					V_{os} at Any Channel		8	
Signal Crosstalk (Frequency at −40 dB)	5●	10	1	$20 \log \frac{V_{os}}{V_{is}} = -40$ dB	Between Any 2 Channels▲		1	MHz
					Between Sections CD4097 Only	Measured on Common	10	
						Measured on Any Channel	18	
Address-or-Inhibit-to-Signal Crosstalk	–	10	10*	V_{SS}=0, t_r,t_f=20 ns, $V_C = V_{DD} - V_{SS}$ (Square Wave)			75	mV (Peak)

● Peak-to-peak voltage symmetrical about $\frac{V_{DD}-V_{SS}}{2}$

▲ Worst case.

* Both ends of channel.

TEST CIRCUITS (Cont'd)

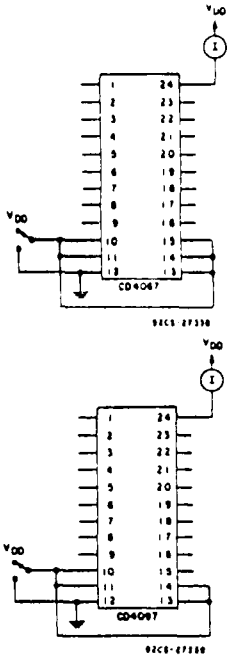


Fig. 10– Quiescent device current.

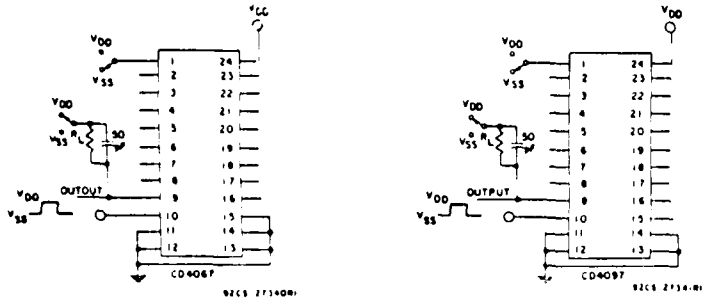


Fig. 11– Turn-on and turn-off propagation delay–address select input to signal output (e.g. measured on channel 0).

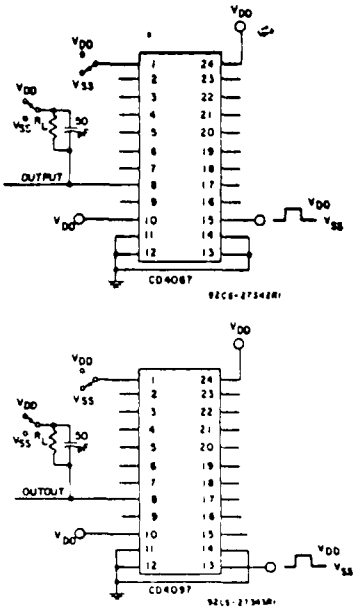


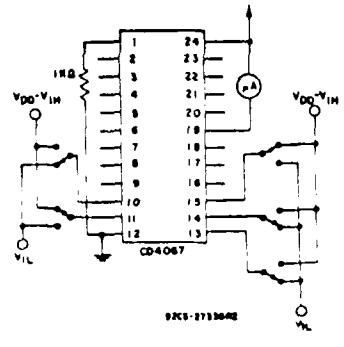
Fig. 12– Turn-on and turn-off propagation delay–inhibit input to signal output (e.g. measured on channel 1).

ELECTRICAL CHARACTERISTICS (Cont'd)

CHARACTERISTIC	CONDITIONS			LIMITS at Indicated Temperature (°C) Values at -55, +25, +125 Apply to D, F, K, H, pkg. Values at -40, +25, +85, apply to E pkg							Units
	V_{is} (V)	V_{SS} (V)	V_{DD} (V)	-55	-40	+85	+125	+25 Min.	+25 Typ.	+25 Max.	
Input Current, I_{IN} Max.	V_{IN} = 0, 18 V		18	±0.1	±0.1	±1	±1	–	$±10^{-5}$	±0.1	μA
Propagation Delay Time: Address or Inhibit-to-Signal OUT (Channel turning ON)	R_L = 10 kΩ, C_L = 50 pF, t_r, t_f = 20 ns	0	5	–	–	–	–	–	325	650	ns
		0	10	–	–	–	–	–	135	270	
		0	15	–	–	–	–	–	95	190	
Address or Inhibit to Signal OUT (Channel turning OFF)	R_L = 300 Ω, C_L = 50 pF, t_r, t_f = 20 ns	0	5	–	–	–	–	–	220	440	ns
		0	10	–	–	–	–	–	90	180	
		0	15	–	–	–	–	–	65	130	
Input Capacitance, C_{IN}	Any Address or Inhibit Input			–	–	–	–	–	5	7.5	pF

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY-VOLTAGE RANGE, (V_{DD})
(Voltages referenced to V_{SS} Terminal) . . . . . -0.5 to +20 V
INPUT VOLTAGE RANGE, ALL INPUTS . . . . . -0.5 to V_{DD} +0.5 V
DC INPUT CURRENT, ANY ONE INPUT . . . . . ±10 mA
POWER DISSIPATION PER PACKAGE (P_D):
For T_A = -40 to +60°C (PACKAGE TYPE E) . . . . . 500 mW
For T_A = +60 to +85°C (PACKAGE TYPE E) . . . . . Derate Linearly at 12 mW/°C to 200 mW
For T_A = -55 to +100°C (PACKAGE TYPES D, F, K) . . . . . 500 mW
For T_A = +100 to +125°C (PACKAGE TYPES D, F, K) . . . . Derate Linearly at 12 mW/°C to 200 mW
DEVICE DISSIPATION PER OUTPUT TRANSISTOR
FOR T_A = FULL PACKAGE-TEMPERATURE RANGE (All Package Types) . . . . . 100 mW
OPERATING-TEMPERATURE RANGE (T_A):
PACKAGE TYPES D, F, K, H . . . . . -55 to +125°C
PACKAGE TYPE E . . . . . -40 to +85°C
STORAGE TEMPERATURE RANGE (T_{stg}) . . . . . -65 to +150°C
LEAD TEMPERATURE (DURING SOLDERING):
At distance 1/16 ± 1/32 inch (1.59 ± 0.79 mm) from case for 10 s max. . . . . +265°C



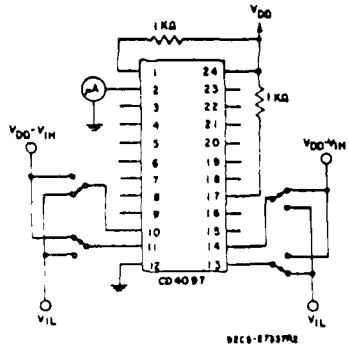
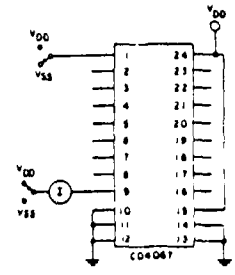


Fig. 8– Input voltage–measure < 2 μA on all OFF channels (e.g., channel 12).

TEST CIRCUITS



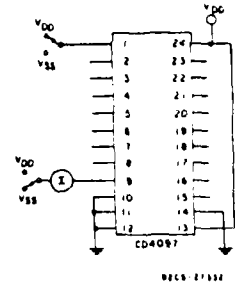
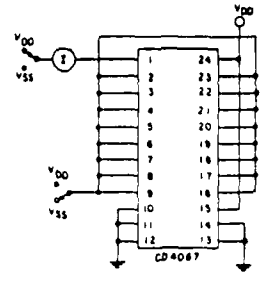


Fig. 7–OFF channel leakage current–any channel OFF.



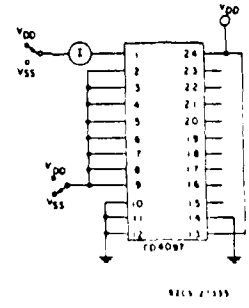


Fig. 9–OFF channel leakage current–all channels OFF

ELECTRICAL CHARACTERISTICS

CHARACTERISTIC	CONDITIONS			LIMITS at Indicated Temperature (°C) Values at −55, +25, +125 Apply to D, F, K, H pkg Values at −40, +25, +85, apply to E pkg							Units
	V_{IS} (V)	V_{SS} (V)	V_{DD} (V)	−55	−40	+85	+125	+25 Min.	+25 Typ.	+25 Max.	
SIGNAL INPUTS (V_{IS}) AND OUTPUTS (V_{OS})											
Quiescent Device Current, I_{DD} Max.			5	5	5	150	150	–	0.04	5	µA
			10	10	10	300	300	–	0.04	10	
			15	20	20	600	600	–	0.04	20	
			20	100	100	3000	3000	–	0.08	100	
ON-state Resistance $V_{SS} \leq V_{IS} \leq V_{DD}$ r_{on} Max		0	5	800	850	1200	1300	–	470	1050	Ω
		0	10	310	330	520	550	–	180	400	
		0	15	200	210	300	320	–	125	240	
Change in on-state Resistance (Between Any Two Channels) Δr_{on}		0	5	–	–	–	–	–	15	–	Ω
		0	10	–	–	–	–	–	10	–	
		0	15	–	–	–	–	–	5	–	
OFF Channel Leakage Current, Any Channel OFF Max. or All Channels OFF (Common OUT/IN) Max		0	18	±100*		±1000*		–	±0.1	±100*	nA
Capacitance: Input, C_{IS}		−5	5	–	–	–	–	–	5	–	pF
Output, C_{OS} CD4067				–	–	–	–	–	55	–	
CD4097				–	–	–	–	–	35		
Feed through, C_{IOS}				–	–	–	–	–	0.2		
Propagation Delay Time (Signal Input to Output	V_{DD}	R_L = 200 KΩ C_L=50 pF t_r, t_f=20 ns	5	–	–	–	–	–	30	60	ns
			10	–	–	–	–	–	15	30	
			15	–	–	–	–	–	10	20	
CONTROL (ADDRESS or INHIBIT) V_C											
Input Low Voltage, V_{IL} Max.	=V_{DD} thru 1 KΩ	R_L=1 KΩ to V_{SS} I_{IS}<2 µA on all OFF Channels	5	1.5				–	–	1.5	V
			10	3				–	–	3	
			15	4				–	–	4	
Input High Voltage, V_{IH} Min.			5	3.5				3.5	–	–	
			10	7				7	–	–	
			15	11				11	–	–	

* Determined by minimum feasible leakage measurement for automatic testing

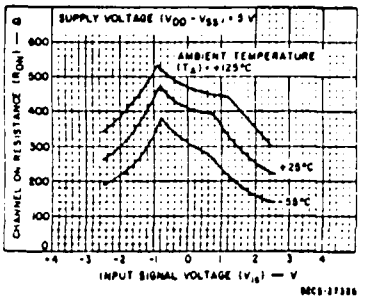


Fig. 3—Typical ON resistance vs. input signal voltage (all types).

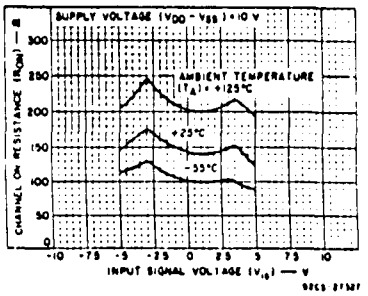


Fig. 4—Typical ON resistance vs. input signal voltage (all types).

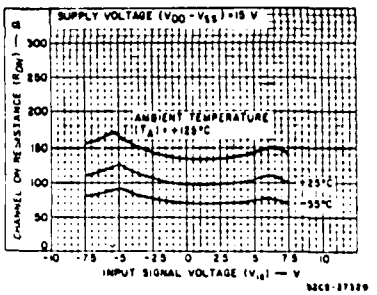


Fig. 5—Typical ON resistance vs. input signal voltage (all types).

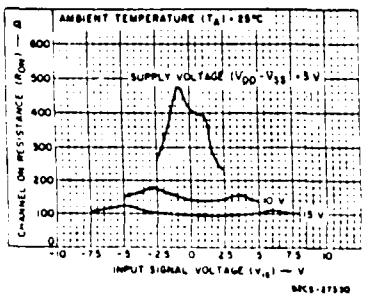


Fig. 6—Typical ON resistance vs. input signal voltage (all types).

CMOS Analog Multiplexers/Demultiplexers

High-Voltage Types (20-Volt Rating)

CD4067B – Single 16-Channel Multiplexer/Demultiplexer

CD4097B – Differential 8-Channel Multiplexer/Demultiplexer

The RCA-CD4067B and CD4097B CMOS analog multiplexers/demultiplexers* are digitally controlled analog switches having low ON impedance, low OFF leakage current, and internal address decoding. In addition, the ON resistance is relatively constant over the full input-signal range.

The CD4067B is a 16-channel multiplexer with four binary control inputs, A,B,C,D, and an inhibit input, arranged so that any combination of the inputs selects one switch.

The CD4097B is a differential 8-channel multiplexer having three binary control inputs A, B, C, and an inhibit input. The inputs permit selection of one of eight pairs of switches.

A logic "1" present at the inhibit input turns all channels off.

The CD4067 and CD4097 are supplied in 24-lead dual-in-line welded-seal ceramic packages (D suffix), 24-lead dual-in-line frit-seal ceramic packages (F suffix), 24-lead dual-in-line plastic packages (E suffix), 24-lead ceramic flat packages (K suffix), and in chip form (H suffix).

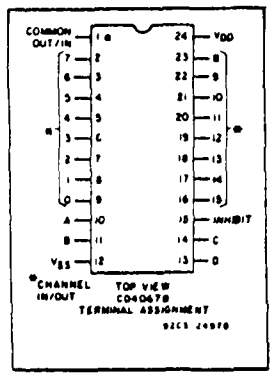
*When these devices are used as demultiplexers, the channel in/out terminals are the outputs and the common out/in terminals are the inputs.

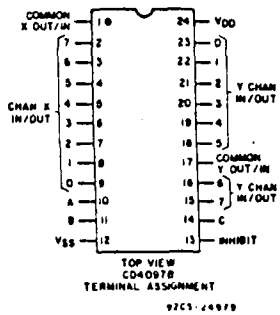
Features:

- Low ON resistance: 125 Ω (typ.) over 15 V_{p-p} signal-input range for $V_{DD}-V_{SS}=15$ V
- High OFF resistance: channel leakage of ±10 pA (typ.) @ $V_{DD}-V_{SS}=10$ V
- Matched switch characteristics: $R_{ON}=5$ Ω (typ.) for $V_{DD}-V_{SS}=15$ V
- Very low quiescent power dissipation under all digital-control input and supply conditions: 0.2 μW (typ.) @ $V_{DD}-V_{SS}=10$ V
- Binary address decoding on chip
- 5-V, 10-V, and 15-V parametric ratings
- 100% tested for quiescent current at 20 V
- Standardized symmetrical output characteristics
- Maximum input current of 1 μA at 18 V over full package temperature range; 100 nA at 18 V and 25°C
- Meets all requirements of JEDEC Tentative Standard No. 13A, "Standard Specifications for Description of 'B' Series CMOS Devices"

Applications:

- Analog and digital multiplexing and demultiplexing
- A/D and D/A conversion
- Signal gating





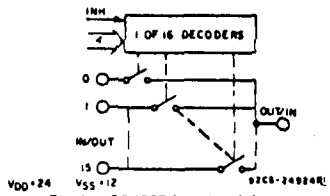


Fig. 1 – CD4067 functional diagram.

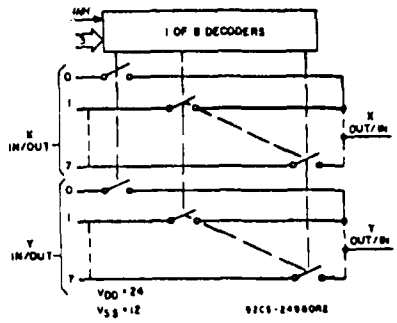


Fig. 2 – CD4097 functional diagram.

Recommended Operating Conditions at T_A = 25°C (Unless Otherwise Specified)

For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges. Values shown apply to all types except as noted.

Characteristic	Min.	Max.	Units
Supply-Voltage Range (T_A=Full Package-Temp. Range)	3	18	V
Multiplexer Switch Input Current Capability	–	25	mA
Output Load Resistance	100	–	Ω

NOTE:

In certain applications, the external load-resistor current may include both V_{DD} and signal-line components. To avoid drawing V_{DD} current when switch current flows into the transmission gate inputs, the voltage drop across the bidirectional switch must not exceed 0.8 volt (calculated from R_{ON} values shown in ELECTRICAL CHARACTERISTICS CHART). No V_{DD} current will flow through R_L if the switch current flows into terminal 1 on the CD4067, terminals 1 and 17 on the CD4097.

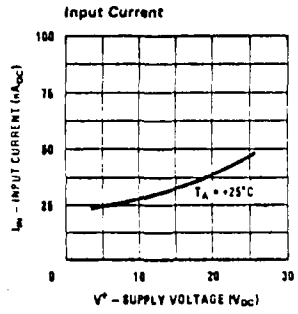
CD4067 TRUTH TABLE

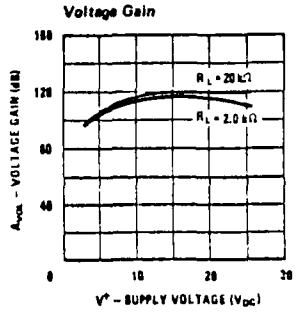
A	B	C	D	Inh	Selected Channel
X	X	X	X	1	None
0	0	0	0	0	0
1	0	0	0	0	1
0	1	0	0	0	2
1	1	0	0	0	3
0	0	1	0	0	4
1	0	1	0	0	5
0	1	1	0	0	6
1	1	1	0	0	7
0	0	0	1	0	8
1	0	0	1	0	9
0	1	0	1	0	10
1	1	0	1	0	11
0	0	1	1	0	12
1	0	1	1	0	13
0	1	1	1	0	14
1	1	1	1	0	15

CD4097 TRUTH TABLE

A	B	C	Inh	Selected Channel
X	X	X	1	None
0	0	0	0	0X, 0Y
1	0	0	0	1X, 1Y
0	1	0	0	2X, 2Y
1	1	0	0	3X, 3Y
0	0	1	0	4X, 4Y
1	0	1	0	5X, 5Y
0	1	1	0	6X, 6Y
1	1	1	0	7X, 7Y

Typical Performance Characteristics (LM2902 only)





Application Hints

The LM124 series are op amps which operate with only a single power supply voltage, have true-differential inputs, and remain in the linear mode with an input common-mode voltage of 0 V_{DC}. These amplifiers operate over a wide range of power supply voltage with little change in performance characteristics. At 25°C amplifier operation is possible down to a minimum supply voltage of 2.3 V_{DC}.

The pinouts of the package have been designed to simplify PC board layouts. Inverting inputs are adjacent to outputs for all of the amplifiers and the outputs have *also been placed at the corners of the package (pins 1,* 7, 8, and 14).

Precautions should be taken to insure that the power supply for the integrated circuit never becomes reversed in polarity or that the unit is not inadvertently installed backwards in a test socket as an unlimited current surge through the resulting forward diode within the IC could cause fusing of the internal conductors and result in a destroyed unit.

Large differential input voltages can be easily accommodated and, as input differential voltage protection diodes are not needed, no large input currents result from large differential input voltages. The differential input voltage may be larger than V^+ without damaging the device. Protection should be provided to prevent the input voltages from going negative more than −0.3 V_{DC} (at 25°C). An input clamp diode with a resistor to the IC input terminal can be used.

To reduce the power supply current drain, the amplifiers have a class A output stage for small signal levels which converts to class B in a large signal mode. This allows the amplifiers to both source and sink large output currents. Therefore both NPN and PNP external current boost transistors can be used to extend the power capability of the basic amplifiers. The output voltage needs to raise approximately 1 diode drop above ground to bias the on-chip vertical PNP transistor for output current sinking applications.

For ac applications, where the load is capacitively coupled to the output of the amplifier, a resistor should be used, from the output of the amplifier to ground to increase the class A bias current and prevent crossover distortion. Where the load is directly coupled, as in dc applications, there is no crossover distortion.

Capacitive loads which are applied directly to the output of the amplifier reduce the loop stability margin. Values of 50 pF can be accommodated using the worst-case non-inverting unity gain connection. Large closed loop gains or resistive isolation should be used if larger load capacitance must be driven by the amplifier.

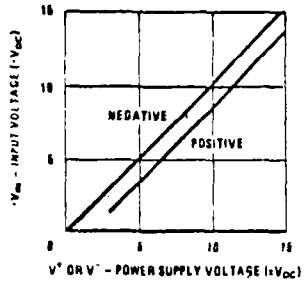
The bias network of the LM124 establishes a drain current which is independent of the magnitude of the power supply voltage over the range of from 3 V_{DC} to 30 V_{DC}.

Output short circuits either to ground or to the positive power supply should be of short time duration. Units can be destroyed, not as a result of the short circuit current causing metal fusing, but rather due to the large increase in IC chip dissipation which will cause eventual failure due to excessive junction temperatures. Putting direct short-circuits on more than one amplifier at a time will increase the total IC power dissipation to destructive levels, if not properly protected with external dissipation limiting resistors in series with the output leads of the amplifiers. The larger value of output source current which is available at 25°C provides a larger output current capability at elevated temperatures (see typical performance characteristics) than a standard IC op amp.

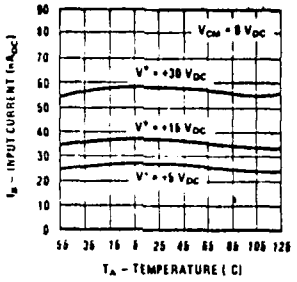
The circuits presented in the section on typical applications emphasize operation on only a single power supply voltage. If complementary power supplies are available, all of the standard op amp circuits can be used. In general, introducing a pseudo-ground (a bias voltage reference of $V^+/2$) will allow operation above and below this value in single power supply systems. Many application circuits are shown which take advantage of the wide input common-mode voltage range which includes ground. In most cases, input biasing is not required and input voltages which range to ground can easily be accommodated.

Typical Performance Characteristics

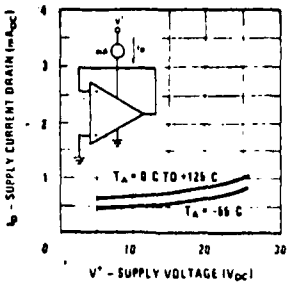
Input Voltage Range



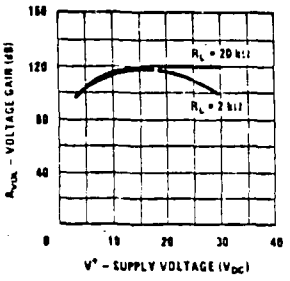
Input Current



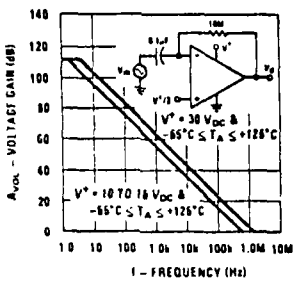
Supply Current



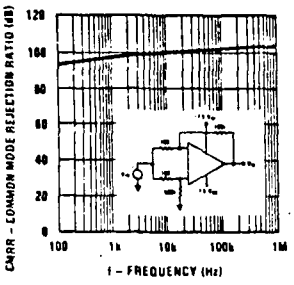
Voltage Gain



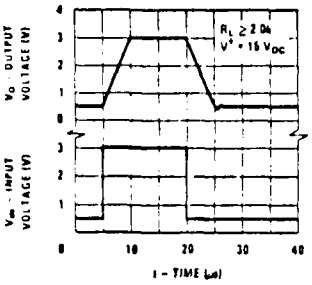
Open Loop Frequency Response



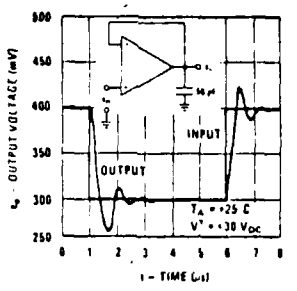
Common Mode Rejection Ratio



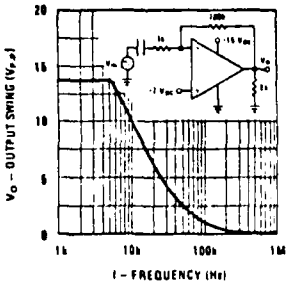
Voltage Follower Pulse Response



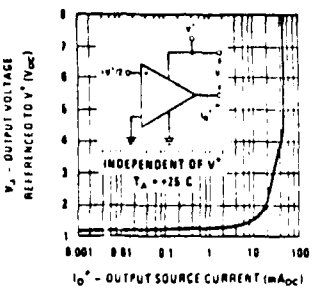
Voltage Follower Pulse Response (Small Signal)



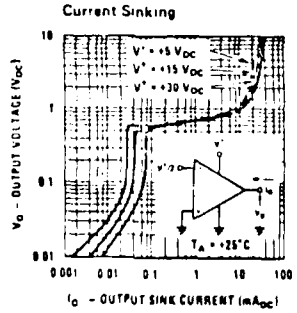
Large Signal Frequency Response



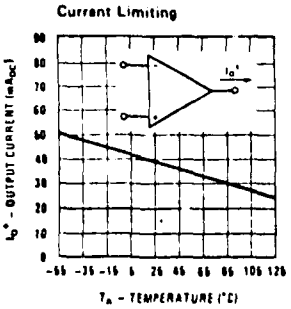
Output Characteristics Current Sourcing



Output Characteristics Current Sinking



Current Limiting



Electrical Characteristics (Continued)

PARAMETER	CONDITIONS	LM124A			LM224A			LM324A			LM124/LM224			LM324			LM2902			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
Input Offset Voltage	(Note 5)			4			4			6			±7			±9			±10	mV_{DC}
Input Offset Voltage Drift	$R_S = 0\Omega$		7	20		7	20		7	30		7			7			7		$\mu V/^\circ C$
Input Offset Current	$I_{IN(+)} - I_{IN(-)}$			30			30			75			±100			±150		45	±200	nA_{DC}
Input Offset Current Drift			10	200		10	200		10	300		10			10			10		$pA_{DC}/^\circ C$
Input Bias Current	$I_{IN(+)}$ or $I_{IN(-)}$		40	100		40	100		40	200		40	300		40	500		40	500	nA_{DC}
Input Common Mode Voltage Range (Note 7)	$V^+ = 30\ V_{DC}$	0		V^+-2	0		V^+-2	0		V^+-2	0		V^+-2	0		V^+-2	0		V^+-2	V_{DC}
Large Signal Voltage Gain	$V^+ = +15\ V_{DC}$ (For Large V_O Swing) $R_L \geq 2\ k\Omega$	25			25			15			25			15			15			V/mV
Output Voltage Swing																				
V_{OH}	$V^+ = +30\ V_{DC}$, $R_L = 2\ k\Omega$	26			26			26			26			26			22			V_{DC}
	$R_L \geq 10\ k\Omega$	27	28		27	28		27	28		27	28		27	28		23	24		V_{DC}
V_{OL}	$V^+ = 5\ V_{DC}$, $R_L \leq 10\ k\Omega$		5	20		5	20		5	20		5	20		5	20		5	100	mV_{DC}
Output Current																				
Source	$V_{IN}^+ = +1\ V_{DC}$, $V_{IN}^- = 0\ V_{DC}$, $V^+ = 15\ V_{DC}$	10	20		10	20		10	20		10	20		10	20		10	20		mA_{DC}
Sink	$V_{IN}^- = +1\ V_{DC}$, $V_{IN}^+ = 0\ V_{DC}$, $V^+ = 15\ V_{DC}$	10	15		5	8		5	8		5	8		5	8		5	8		mA_{DC}
Differential Input Voltage	(Note 7)			32			32			32			32			32			26	V_{DC}

Note 1: For operating at high temperatures, the LM324/LM324A, LM2902 must be derated based on a +125°C maximum junction temperature and a thermal resistance of 175°C/W which applies for the device soldered in a printed circuit board, operating in a still air ambient. The LM224/LM224A and LM124/LM124A can be derated based on a +150°C maximum junction temperature. The dissipation is the total of all four amplifiers—use external resistors, where possible, to allow the amplifier to saturate or to reduce the power which is dissipated in the integrated circuit.

Note 2: Short circuits from the output to V^+ can cause excessive heating and eventual destruction. The maximum output current is approximately 40 mA independent of the magnitude of V^+. At values of supply voltage in excess of +15 V_{DC}, continuous short-circuits can exceed the power dissipation ratings and cause eventual destruction. Destructive dissipation can result from simultaneous shorts on all amplifiers.

Note 3: This input current will only exist when the voltage at any of the input leads is driven negative. It is due to the collector-base junction of the input PNP transistors becoming forward biased and thereby acting as input diode clamps. In addition to this diode action, there is also lateral NPN parasitic transistor action on the IC chip. This transistor action can cause the output voltages of the op amps to go to the V^+ voltage level (or to ground for a large overdrive) for the time duration that an input is driven negative. This is not destructive and normal output states will re-establish when the input voltage, which was negative, again returns to a value greater than −0.3 V_{DC} (at 25°C).

Note 4: These specifications apply for $V^+ = +5\ V_{DC}$ and −55°C ≤ T_A ≤ +125°C, unless otherwise stated. With the LM224/LM224A, all temperature specifications are limited to −25°C ≤ T_A ≤ +85°C, the LM324/LM324A temperature specifications are limited to 0°C ≤ T_A ≤ +70°C, and the LM2902 specifications are limited to −40°C ≤ T_A ≤ +85°C.

Note 5: $V_O \cong 1.4\ V_{DC}$, $R_S = 0\Omega$ with V^+ from 5 V_{DC} to 30 V_{DC}; and over the full input common-mode range (0 V_{DC} to $V^+ - 1.5\ V_{DC}$).

Note 6: The direction of the input current is out of the IC due to the PNP input stage. This current is essentially constant, independent of the state of the output so no loading change exists on the input lines.

Note 7: The input common-mode voltage of either input signal voltage should not be allowed to go negative by more than 0.3V (at 25°C). The upper end of the common-mode voltage range is $V^+ - 1.5V$, but either or both inputs can go to +32 V_{DC} without damage (+26 V_{DC} for LM2902).

Note 8: Due to proximity of external components, insure that coupling is not originating via stray capacitance between these external parts. This typically can be detected as this type of capacitive increases at higher frequencies.

Absolute Maximum Ratings

	LM124/LM224/LM324 LM124A/LM224A/LM324A	LM2902
Supply Voltage, V^+	32 V_{DC} or ±16 V_{DC}	26 V_{DC} or ±13 V_{DC}
Differential Input Voltage	32 V_{DC}	26 V_{DC}
Input Voltage	−0.3 V_{DC} to +26 V_{DC}	−0.3 V_{DC} to +26 V_{DC}
Power Dissipation (Note 1)		
Molded DIP	570 mW	570 mW
Cavity DIP	900 mW	
Flat Pack	800 mW	
Output Short Circuit to GND (One Amplifier) (Note 2) $V^+ \leq 15\ V_{DC}$ and $T_A = 25^\circ C$	Continuous	Continuous

	LM124/LM224/LM324 LM124A/LM224A/LM324A	LM2902
Input Current ($V_{IN} < -0.3\ V_{DC}$) (Note 3)	50 mA	50 mA
Operating Temperature Range		−40°C to +85°C
LM324/LM324A	0°C to +70°C	
LM224/LM224A	−25°C to +85°C	
LM124/LM124A	−55°C to +125°C	
Storage Temperature Range	−65°C to +150°C	−65°C to +150°C
Lead Temperature (Soldering, 10 seconds)	300°C	300°C

Electrical Characteristics ($V^+ = +5.0\ V_{DC}$, Note 4)

PARAMETER	CONDITIONS	LM124A			LM224A			LM324A			LM124/LM224			LM324			LM2902			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
Input Offset Voltage	$T_A = 25^\circ C$, (Note 5)		1	2		1	3		2	3		±2	±5		±2	±7		±2	±7	mV_{DC}
Input Bias Current (Note 6)	$I_{IN(+)}$ or $I_{IN(-)}$, $T_A = 25^\circ C$		20	50		40	80		45	100		45	150		45	250		45	250	nA_{DC}
Input Offset Current	$I_{IN(+)} - I_{IN(-)}$, $T_A = 25^\circ C$		2	10		2	15		5	30		±3	±30		±5	±50		±5	±50	nA_{DC}
Input Common Mode Voltage Range (Note 7)	$V^+ = 30\ V_{DC}$, $T_A = 25^\circ C$	0		$V^+-1.5$	0		$V^+-1.5$	0		$V^+-1.5$	0		$V^+-1.5$	0		$V^+-1.5$	0		$V^+-1.5$	V_{DC}
Supply Current	$R_L = \infty$, $V_{CC} = 30V$, (LM2902 $V_{CC} = 26V$)		1.5	3		1.5	3		1.5	3		1.5	3		1.5	3		1.5	3	mA_{DC}
	$R_L = \infty$ On All Op Amps Over Full Temperature Range		0.7	1.2		0.7	1.2		0.7	1.2		0.7	1.2		0.7	1.2		0.7	1.2	mA_{DC}
Large Signal Voltage Gain	$V^+ = 15\ V_{DC}$ (For Large V_O Swing) $R_L \geq 2\ k\Omega$, $T_A = 25^\circ C$	50	100		50	100		25	100		50	100		25	100			100		V/mV
Output Voltage Swing	$R_L = 2\ k\Omega$, $T_A = 25^\circ C$ (LM2902 $R_L \geq 10\ k\Omega$)	0		$V^+-1.5$	0		$V^+-1.5$	0		$V^+-1.5$	0		$V^+-1.5$	0		$V^+-1.5$	0		$V^+-1.5$	V_{DC}
Common Mode Rejection Ratio	DC, $T_A = 25^\circ C$	70	85		70	85		65	85		70	85		65	70		50	70		dB
Power Supply Rejection Ratio	DC, $T_A = 25^\circ C$	65	100		65	100		65	100		65	100		65	100		50	100		dB
Amplifier to Amplifier Coupling (Note 8)	f = 1 kHz to 20 kHz, $T_A = 25^\circ C$ (Input Referred)		−120			−120			−120			−120			−120			−120		dB
Output Current																				
Source	$V_{IN}^+ = 1\ V_{DC}$, $V_{IN}^- = 0\ V_{DC}$, $V^+ = 15\ V_{DC}$, $T_A = 25^\circ C$	20	40		20	40		20	40		20	40		20	40		20	40		mA_{DC}
Sink	$V_{IN}^- = 1\ V_{DC}$, $V_{IN}^+ = 0\ V_{DC}$, $V^+ = 15\ V_{DC}$, $T_A = 25^\circ C$	10	20		10	20		10	20		10	20		10	20		10	20		mA_{DC}
	$V_{IN}^- = 1\ V_{DC}$, $V_{IN}^+ = 0\ V_{DC}$, $T_A = 25^\circ C$, $V_O = 200\ mV_{DC}$	12	50		12	50		12	50		12	50		12	50					μA_{DC}
Short Circuit to Ground	$T_A = 25^\circ C$, (Note 2)		40	60		40	60		40	60		40	60		40	60		40	60	mA_{DC}

National Semiconductor

Operational Amplifiers/Buffers

LM124/LM224/LM324, LM124A/LM224A/LM324A, LM2902 Low Power Quad Operational Amplifiers

General Description

The LM124 series consists of four independent, high gain, internally frequency compensated operational amplifiers which were designed specifically to operate from a single power supply over a wide range of voltages. Operation from split power supplies is also possible and the low power supply current drain is independent of the magnitude of the power supply voltage.

Application areas include transducer amplifiers, dc gain blocks and all the conventional op amp circuits which now can be more easily implemented in single power supply systems. For example, the LM124 series can be directly operated off of the standard +5 V_{DC} power supply voltage which is used in digital systems and will easily provide the required interface electronics without requiring the additional ±15 V_{DC} power supplies.

Unique Characteristics

- In the linear mode the input common-mode voltage range includes ground and the output voltage can also swing to ground, even though operated from only a single power supply voltage.
- The unity gain cross frequency is temperature compensated.
- The input bias current is also temperature compensated.

Advantages

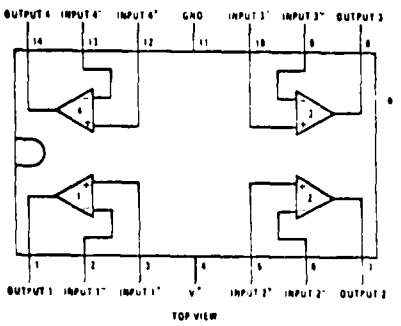
- Eliminates need for dual supplies
- Four internally compensated op amps in a single package
- Allows directly sensing near GND and V_{OUT} also goes to GND
- Compatible with all forms of logic
- Power drain suitable for battery operation

Features

- Internally frequency compensated for unity gain
- Large dc voltage gain 100 dB
- Wide bandwidth (unity gain) (temperature compensated) 1 MHz
- Wide power supply range:
  - Single supply 3 V_{DC} to 30 V_{DC}
  - or dual supplies ±1.5 V_{DC} to ±15 V_{DC}
- Very low supply current drain (800μA) – essentially independent of supply voltage (1 mW/op amp at +5 V_{DC})
- Low input biasing current (temperature compensated) 45 nA_{DC}
- Low input offset voltage 2 mV_{DC}
  and offset current 5 nA_{DC}
- Input common-mode voltage range includes ground
- Differential input voltage range equal to the power supply voltage
- Large output voltage swing 0 V_{DC} to V^+ – 1.5 V_{DC}

Connection Diagram

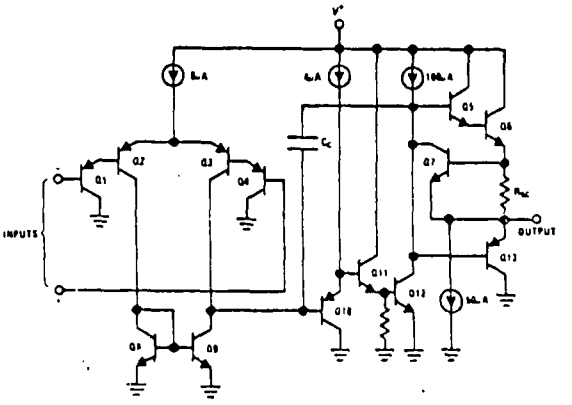
Dual-In-Line Package



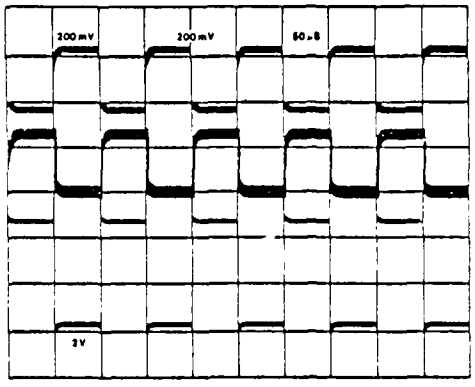
Order Number LM124J, LM124AJ, LM224J, LM224AJ, LM324J, LM324AJ or LM2902J
See NS Package J14A

Order Number LM324N, LM324AN or LM2902N
See NS Package N14A

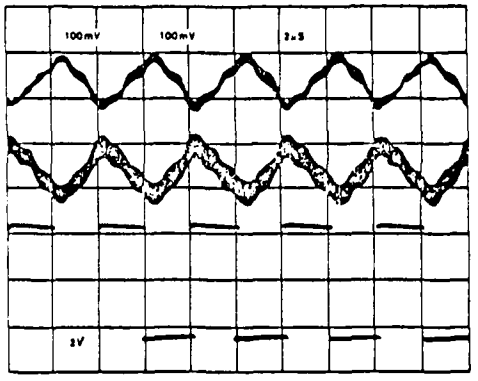
Schematic Diagram (Each Amplifier)



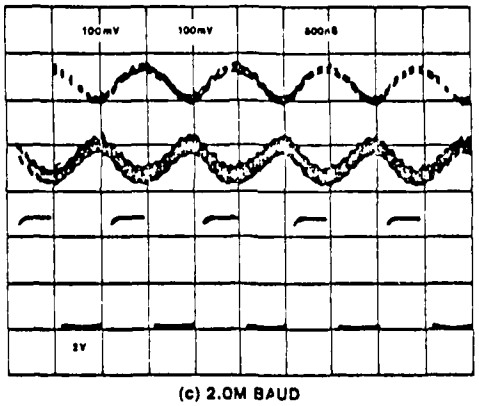
PHASE COMPARATOR (PINS 4 AND 5) AND FSK (PIN 16) OUTPUTS FOR DATA RATES OF



(a) 20K BAUD



(b) 500K BAUD



(c) 2.0M BAUD

NOTE
Top trace-pin 4
Center trace-pin 5
Bottom trace-pin 16

Figure 6

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The loop filter diagram shown is explained by the following equation:

$$F(s) = \frac{1}{1 + sRC_3} \qquad \text{Equation 5}$$

$R = R_{12} = R_{13} = 1.3k\Omega$ (INTERNAL)

By adding capacitors to pins 4 and 5, two poles are added to the loop transfer function at $\omega = \frac{1}{RC_3}$.

APPLICATIONS

FM DEMODULATOR

The NE564 can be used as an FM demodulator. The connections for operation at 5V and 12V are shown in figures 2 and 3 respectively. The input signal is ac coupled with the output signal being extracted at pin 14. Loop filtering is provided by the capacitors at pins 4 and 5 with additional filtering being provided by the capacitor at pin 14. Since the conversion gain of the VCO is not very high, to obtain sufficient demodulated output signal the frequency deviation in the input signal should be 1% or higher.

MODULATION TECHNIQUES

The NE564 phase locked loop can be modulated at either the loop filter ports (pins 4 and 5) or the input port (pin 6) as shown in figure 4. The approximate modulation frequency can be determined from the frequency conversion gain curve shown in figure 5. This curve will be appropriate for signals injected into pins 4 and 5 as shown in figure 4.

FSK Demodulation

The 564 PLL is particularly attractive for FSK demodulation since it contains an internal voltage comparator and VCO which have TTL compatible inputs and outputs, and it can operate from a single 5 volt power supply. Demodulated dc voltages associated with the mark and space frequencies are recovered with a single external capacitor in a dc retriever without utilizing extensive filtering networks. An internal comparator, acting as a Schmitt trigger with an adjustable hysteresis, shapes the demodulated voltages into compatible TTL output levels. The high frequency design of the 564 enables it to demodulate FSK at high data rates in excess of 1.0M baud.

Figure 5 shows a high-frequency FSK decoder designed for input frequency deviations of ± 1.0MHz centered around a free-running frequency of 10.8MHz. The value of the timing capacitance required was estimated from figure 8 to be approximately 40pF. A trimmer capacitor was added to fine tune f_o' to 10.8MHz.

The lock range graph indicates that the ± 1.0MHz frequency deviations will be within the lock range for input signal levels greater than approximately 50mV with zero pin 2 bias current. While strictly this figure is appropriate only for 5MHz, it can be used as a guide for lock range estimates at other f_o' frequencies.

The hysteresis was adjusted experimentally via the 10kΩ potentiometer and 2kΩ bias arrangement to give the waveshape shown in figure 7 for 20K, 500K, 2M baud rates with square wave FSK modulation. Note the magnitude and phase relationships of the phase comparators output voltages with respect to each other and to the FSK output. The high frequency sum components of the input and VCO frequency also are visible as noise on the phase comparators outputs.

10.8MHz FSK DECODER USING THE 564

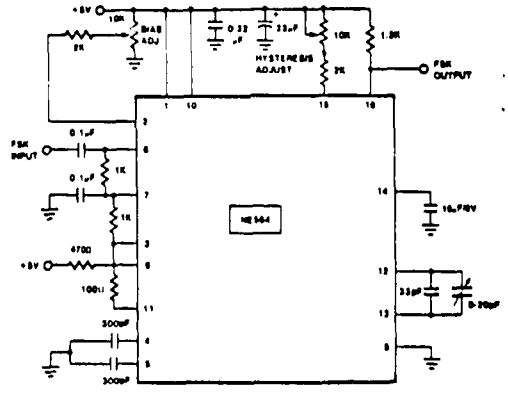

Figure 5

temperature coefficient due to the positive temperature coefficient of the monolithic resistor. To compensate for this, a current I_R with negative temperature coefficient is introduced to achieve a low frequency drift with temperature.

Phase Comparator Section

The phase comparator consists of a double balanced modulator with a limiter amplifier to improve AM rejection. Schottky clamped vertical PNPs are used to obtain TTL level inputs. The loop gain can be varied by changing the current in Q_4 and Q_{15} which effectively changes the gain of the differential amplifiers. This can be accomplished by introducing a current at pin 2.

Post Detection Processor Section

The post detection processor consists of a unity gain transconductance amplifier and comparator. The amplifier can be used as a dc retriever for demodulation of FSK signals, and as a post detection filter for linear FM demodulation. The comparator has adjustable hysteresis so that phase jitter in the output signal can be eliminated.

As shown in the equivalent schematic, the dc retriever is formed by the transductance amplifier Q_{42}–Q_{43} together with an external capacitor which is connected at the amplifier output (pin 14). This forms an integrator whose output voltage is shown in the following equation:

$$V_O = \frac{g_m}{C_2} \int V_{in} dt \qquad \text{Equation 3}$$

g_m = transconductance of the amplifier
C_2 = capacitor at the output (pin 14)
V_{in} = signal voltage at amplifier input

With proper selection of C_2, the integrator time constant can be varied so that the output voltage is the dc or average value of the input signal for use in FSK, or as a post detection filter in linear demodulation.

The comparator with hysteresis is made up of Q_{49}–Q_{50} with positive feedback being provided by Q_{47}-Q_{48}. The hysteresis is varied by changing the current in Q_{52} with a resulting variation in the loop gain of the comparator. This method of hysteresis control, which is a dc control, provides symmetric variation around the nominal value.

Design Formula

The free running frequency of the VCO is shown by the following equation:

$$f_o \approx \frac{1}{25\, R_C\, (C_1 + C_S)} \qquad \text{Equation 4}$$

R_C = 100Ω
C_1 = external cap in farads
C_S = stray capacitance

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FM DEMODULATOR AT 5V

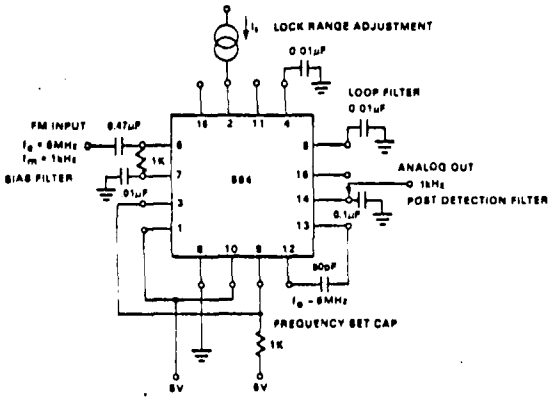


Figure 2

FM DEMODULATOR AT 12V

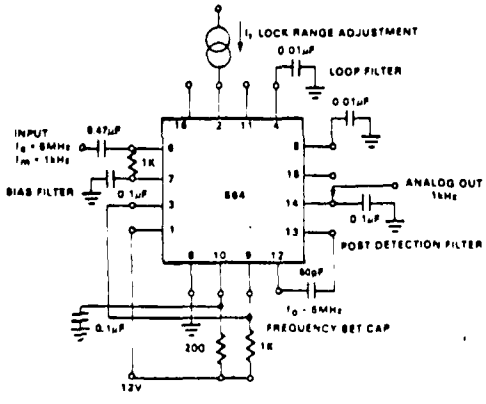


Figure 3

MODULATOR

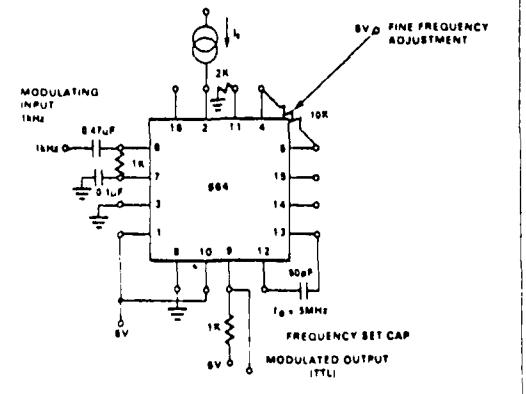


Figure 4

FUNCTIONAL DESCRIPTION (figure 1)

The NE564 is a monolithic phase locked loop with a post detection processor. The use of Schottky clamped transistors and optimized device geometries extends the frequency of operation to greater than 50MHz. In addition to the classical PLL applications, the NE564 can be used as a modulator with a controllable frequency deviation.

The output voltage of the PLL can be written as shown in the following equation:

$$V_O = \frac{(f_{in} - f_o)}{K_{VCO}} \qquad \text{Equation 1}$$

K_{VCO} = conversion gain of the VCO
f_{in} = frequency of the input signal
f_o = free running frequency of the VCO

The process of recovering FSK signals involves the conversion of the PLL output into logic compatible signals. For high data rates, a considerable amount of carrier will be present at the output of the PLL due to the wideband nature of the loop filter. To avoid the use of complicated filters, a comparator with hysteresis or Schmitt trigger is required. With the conversion gain of the VCO fixed, the output voltage as given by Equation 1 varies according to the frequency deviation of f_{in} from f_o. Since this differs from system to system, it is necessary that the hysteresis of the Schmitt trigger be capable of being changed, so that it can be optimized for a particular system. This is accomplished in the 564 by varying the voltage at pin 15 which results in a change of the hysteresis of the Schmitt trigger.

For FSK signals, an important factor to be considered is the drift in the free running frequency of the VCO itself. If this changes due to temperature, according to Equation 1 it will lead to a change in the dc levels of the PLL output, and consequently to errors in the digital output signal. This is especially true for narrow band signals where the deviation in f_{in} itself may be less than the change in f_o due to temperature. This effect can be eliminated if the dc or average value of the signal is retrieved and used as the reference to the comparator. In this manner, variations in the dc levels of the PLL output do not affect the FSK output.

VCO Section

Due to its inherent high frequency performance, an emitter coupled oscillator is used in the VCO. In the circuit, shown in the equivalent schematic, transistors Q_{21} and Q_{23} with current sources Q_{25}–Q_{26} form the basic oscillator. The free running frequency of the oscillator is shown in the following equation:

$$f_o \approx \frac{1}{25\, R_C (C_1 + C_S)} \qquad \text{Equation 2}$$

$R_C = R_{19} = R_{20} = 100\Omega$ (INTERNAL)
C_1 = external frequency setting capacitor
C_S = stray capacitance

Variation of V_d (phase detector output voltage) changes the frequency of the oscillator. As indicated by Equation 2, the frequency of the oscillator has a negative

EQUIVALENT SCHEMATIC

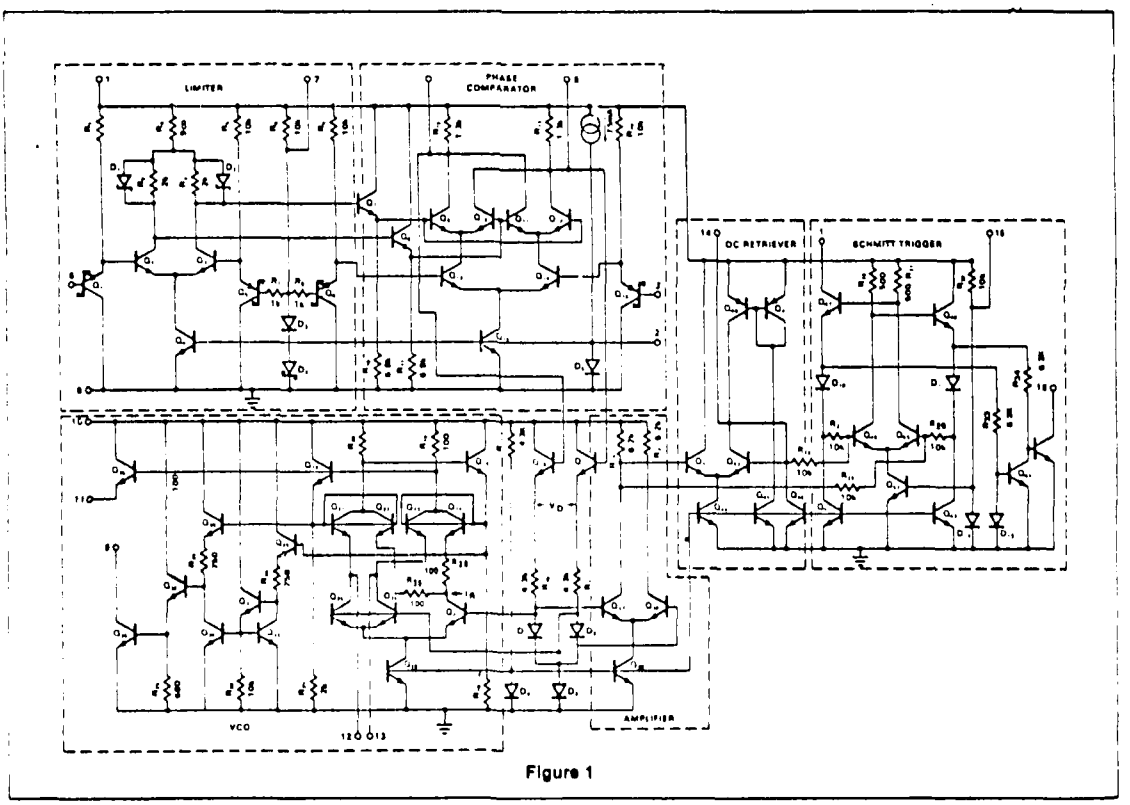


Figure 1

CMOS Ripple-Carry Binary Counter/Dividers

High-Voltage Types (20-Volt Rating)

CD4020B – 14 Stage
CD4024B – 7 Stage
CD4040B – 12 Stage

RCA-CD4020B, CD4024B, and CD4040B are ripple-carry binary counters. All counter stages are master-slave flip-flops. The state of a counter advances one count on the negative transition of each input pulse; a high level on the RESET line resets the counter to its all zeros state. Schmitt trigger action on the input pulse line permits unlimited rise and fall times. All inputs and outputs are buffered.

The CD4020B and CD4040B types are supplied in 16-lead hermetic dual-in-line ceramic packages (D and F suffixes), 16-lead dual-in-line plastic packages (E suffix), 16-lead ceramic flat packages (K suffix), and in chip form (H suffix).

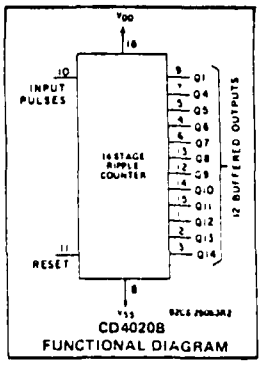
The CD4024B types are supplied in 14-lead hermetic dual-in-line ceramic packages (D and F suffixes), 14-lead dual-in-line plastic packages (E suffix), 14-lead ceramic flat packages (K suffix), and in chip form (H suffix).

Features:

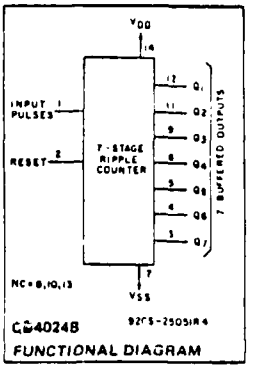
- Medium-speed operation
- Fully static operation
- Buffered inputs and outputs
- 100% tested for quiescent current at 20 V
- Standardized, symmetrical output characteristics
- Fully static operation
- Common reset
- 5-V, 10-V, and 15-V parametric ratings
- Maximum input current of 1 μA at 18 V over full package-temperature range; 100 nA at 18 V and 25°C
- Noise margin (over full package-temperature range): 1 V at V_{DD} = 5 V; 2 V at V_{DD} = 10 V; 2.5 V at V_{DD} = 15 V
- Meets all requirements of JEDEC Tentative Standard No. 13A, "Standard Specifications for Description of 'B' Series CMOS Devices"

Applications:

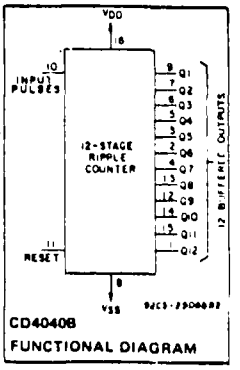
- Control counters
- Timers
- Frequency dividers
- Time-delay circuits



CD4020B
FUNCTIONAL DIAGRAM



CD4024B
FUNCTIONAL DIAGRAM



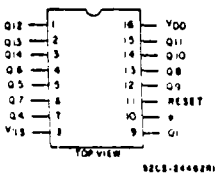
CD4040B
FUNCTIONAL DIAGRAM

MAXIMUM RATINGS, *Absolute-Maximum Values:*

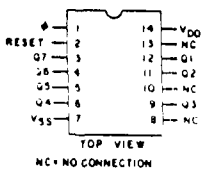
DC SUPPLY-VOLTAGE RANGE, (V_{DD}) (Voltages referenced to V_{SS} Terminal)	−0.5 to +20 V
INPUT VOLTAGE RANGE, ALL INPUTS	−0.5 to V_{DD} +0.5 V
DC INPUT CURRENT, ANY ONE INPUT	±10 mA
POWER DISSIPATION PER PACKAGE (P_D):	
For T_A = −40 to +60°C (PACKAGE TYPE E)	500 mW
For T_A = +60 to +85°C (PACKAGE TYPE E)	Derate Linearly at 12 mW/°C to 200 mW
For T_A = −55 to +100°C (PACKAGE TYPES D, F, K)	500 mW
For T_A = +100 to +125°C (PACKAGE TYPES D, F, K)	Derate Linearly at 12 mW/°C to 200 mW
DEVICE DISSIPATION PER OUTPUT TRANSISTOR FOR T_A = FULL PACKAGE-TEMPERATURE RANGE (All Package Types)	100 mW
OPERATING-TEMPERATURE RANGE (T_A):	
PACKAGE TYPES D, F, K, H	−55 to +125°C
PACKAGE TYPE E	−40 to +85°C
STORAGE TEMPERATURE RANGE (T_{stg})	−65 to +150°C
LEAD TEMPERATURE (DURING SOLDERING):	
At distance 1/16 ± 1/32 inch (1.59 ± 0.79 mm) from case for 10 s max.	+265°C

TERMINAL ASSIGNMENTS

CD4020B

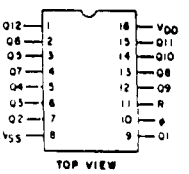


CD4024B



NC = NO CONNECTION

CD4040B



RECOMMENDED OPERATING CONDITIONS at T_A = 25°C, Unless Otherwise Specified

For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC		V_{DD}	Min.	Max.	UNITS
Supply Voltage Range (at T_A = Full Package-Temperature Range)			3	18	V
Input-Pulse Frequency,	f_ϕ	5	–	3.5	MHz
		10	–	8	
		15	–	12	
Input-Pulse Width,	t_W	5	140	–	ns
		10	60	–	
		15	40	–	
Input-Pulse Rise or Fall Time,	$t_{r\phi}$, $t_{f\phi}$	5	Unlimited		μs
		10			
		15			
Reset Pulse Width,	t_W	5	200	–	ns
		10	80		
		15	60		
Reset Removal Time,	t_{REM}	5	350	–	ns
		10	150	–	
		15	100	–	

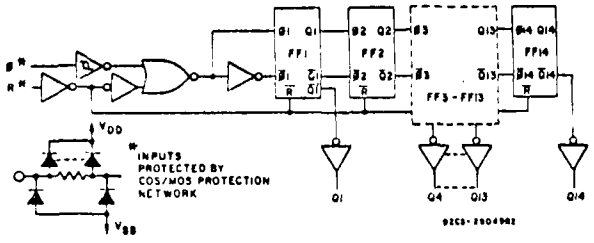


Fig. 1 – Logic diagram for CD4020B.

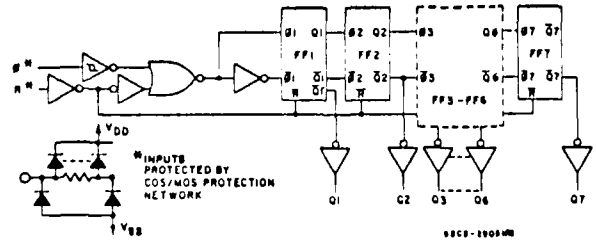


Fig. 2 – Logic diagram for CD4024B.

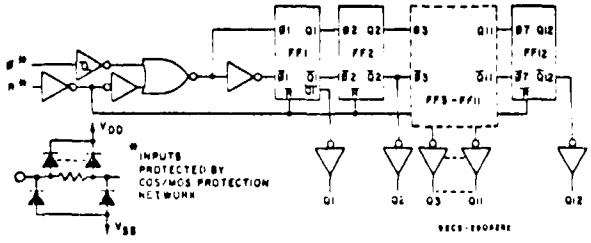


Fig. 3 – Logic diagram for CD4040B.

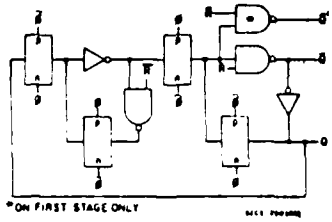


Fig. 4 – Detail of typical flip-flop stage.

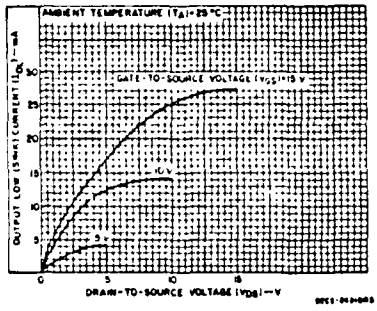


Fig. 5 – Typical output low (sink) current characteristics.

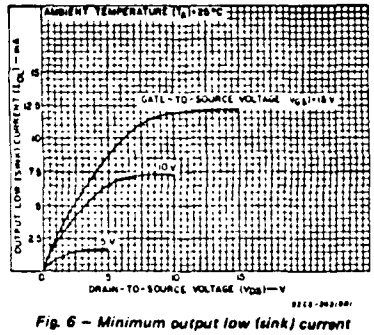


Fig. 6 – Minimum output low (sink) current characteristics.

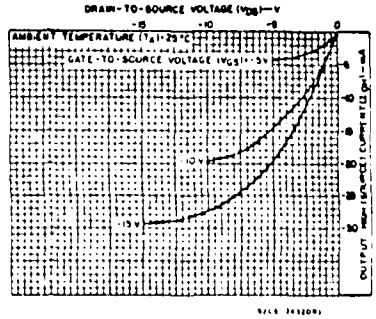


Fig. 7 – Typical output high (source) current characteristics.

STATIC ELECTRICAL CHARACTERISTICS

CHARACTERISTIC	CONDITIONS			LIMITS AT INDICATED TEMPERATURES (°C) Values at -55, +25, +125 Apply to D, F, K, H Packages Values at −40, +25, +85 Apply to E Package							UNITS
									+25		
	V_O (V)	V_{IN} (V)	V_{DD} (V)	−55	−40	+85	+125	Min.	Typ.	Max.	
Quiescent Device Current, I_{DD} Max.	–	0,5	5	5	5	150	150	–	0.04	5	μA
	–	0,10	10	10	10	300	300	–	0.04	10	
	–	0,15	15	20	20	600	600	–	0.04	20	
	–	0,20	20	100	100	3000	3000	–	0.08	100	
Output Low (Sink) Current I_{OL} Min.	0.4	0,5	5	0.64	0.61	0.42	0.36	0.51	1	–	mA
	0.5	0,10	10	1.6	1.5	1.1	0.9	1.3	2.6	–	
	1.5	0,15	15	4.2	4	2.8	2.4	3.4	6.8	–	
Output High (Source) Current, I_{OH} Min.	4.6	0,5	5	-0.64	-0.61	-0.42	-0.36	-0.51	-1	–	
	2.5	0,5	5	-2	-1.8	-1.3	-1.15	-1.6	-3.2	–	
	9.5	0,10	10	-1.6	-1.5	-1.1	-0.9	-1.3	-2.6	–	
	13.5	0,15	15	-4.2	-4	-2.8	-2.4	-3.4	-6.8	–	
Output Voltage: Low-Level, V_{OL} Max.	–	0,5	5	0.05				–	0	0.05	V
	–	0,10	10	0.05				–	0	0.05	
	–	0,15	15	0.05				–	0	0.05	
Output Voltage: High-Level, V_{OH} Min.	–	0,5	5	4.95				4.95	5	–	
	–	0,10	10	9.95				9.95	10	–	
	–	0,15	15	14.95				14.95	15	–	
Input Low Voltage, V_{IL} Max.	0.5, 4.5	–	5	1.5				–	–	1.5	V
	1, 9	–	10	3				–	–	3	
	1.5,13.5	–	15	4				–	–	4	
Input High Voltage, V_{IH} Min.	0.5, 4.5	–	5	3.5				3.5	–	–	
	1, 9	–	10	7				7	–	–	
	1.5,13.5	–	15	11				11	–	–	
Input Current I_{IN} Max.	–	0,18	18	±0.1	±0.1	±1	±1	–	$±10^{-5}$	±0.1	μA

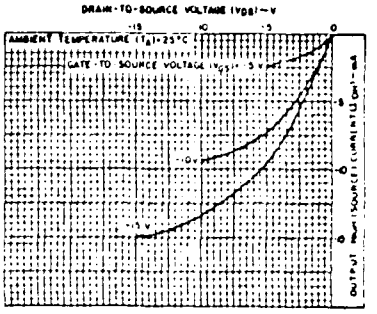


Fig. 8 – Minimum output high (source) current characteristics.

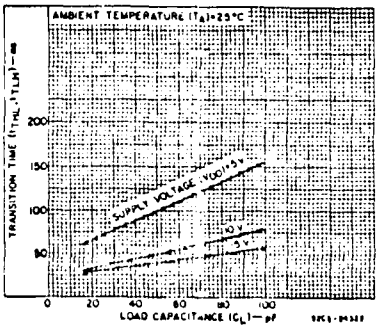
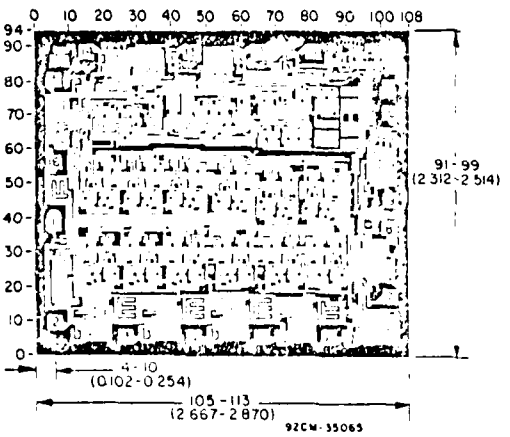
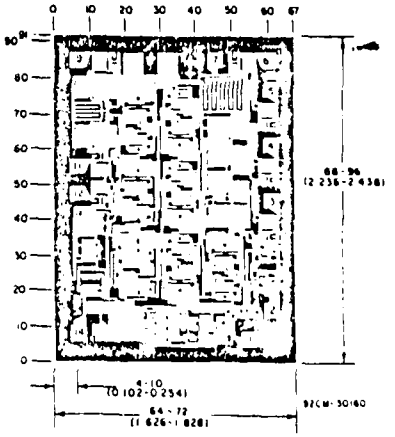


Fig. 9 – Typical transition time as a function of load capacitance.



Dimensions and Pad Layout for CD4020BH. Dimensions and pad layout for CD4040BH are identical.

Dimensions in parentheses are in millimeters and are derived from the basic inch dimensions as indicated. Grid graduations are in mils (10^{-3} inch).



Dimensions and Pad Layout for CD4024BH.

The photographs and dimensions of each CMOS chip represent a chip when it is part of the wafer. When the wafer is separated into individual chips, the angle of cleavage may vary with respect to the chip face for different chips. The actual dimensions of the isolated chip, therefore, may differ slightly from the nominal dimensions shown. The user should consider a tolerance of −3 mils to +16 mils applicable to the nominal dimensions shown.

DYNAMIC ELECTRICAL CHARACTERISTICS at T_A = 25°C, Input t_r, t_f = 20 ns, C_L = 50 pF, R_L = 200 kΩ

CHARACTERISTIC	TEST CONDITIONS	V_{DD} (V)	LIMITS Min.	Typ.	Max.	UNITS
Input-Pulse Operation						
Propagation Delay Time, ϕ to Q_1 Out; t_{PHL}, t_{PLH}		5	–	180	360	ns
		10	–	80	160	
		15	–	65	130	
Q_n to Q_n + 1; t_{PHL}, t_{PLH}		5	–	100	200	ns
		10	–	40	80	
		15	–	30	60	
Transition Time, t_{THL}, t_{TLH}		5	–	100	200	ns
		10	–	50	100	
		15	–	40	80	
Minimum Input-Pulse Width, t_W		5	–	70	140	ns
		10	–	30	60	
		15	–	20	40	
Input-Pulse Rise or Fall Time, $t_{r\phi}$, $t_{f\phi}$		5	Unlimited			μs
		10				
		15				
Maximum Input-Pulse Frequency, f_ϕ		5	3.5	7	–	MHz
		10	8	16	–	
		15	12	24	–	
Input Capacitance, C_I	Any Input		–	5	7.5	pF
Reset Operation						
Propagation Delay Time, t_{PHL}		5	–	140	280	ns
		10	–	60	120	
		15	–	50	100	
Minimum Reset Pulse Width, t_W		5	–	100	200	ns
		10	–	40	80	
		15	–	30	60	
Reset Removal Time, t_{REM}		5	–	175	350	ns
		10	–	75	150	
		15	–	50	100	

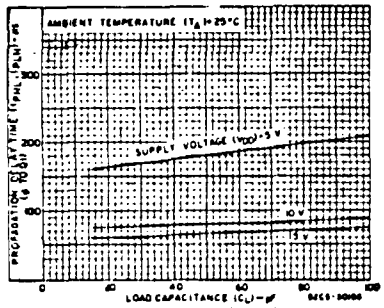


Fig. 10 – Typical propagation delay time as a function of load capacitance (ϕ to Q_1).

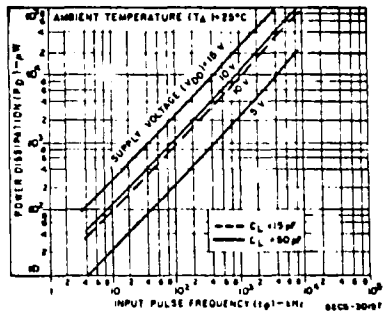


Fig. 11 – Typical dynamic power dissipation as a function of input pulse frequency for CD4020B.

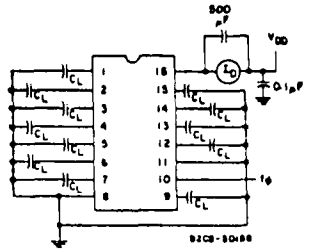


Fig. 12 – Dynamic power dissipation test circuit for CD4020B.

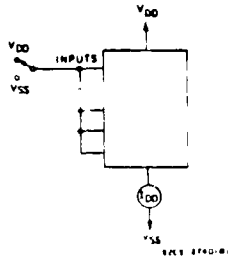


Fig. 13 – Quiescent device current test circuit.

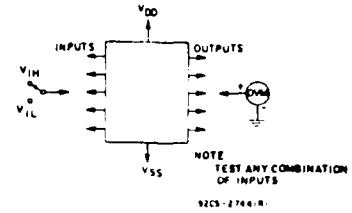


Fig. 14 – Input voltage test circuits.

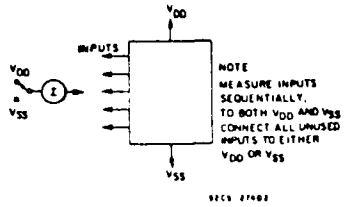


Fig. 15 – Input current test circuit.

CMOS 8-Input NOR/OR Gate

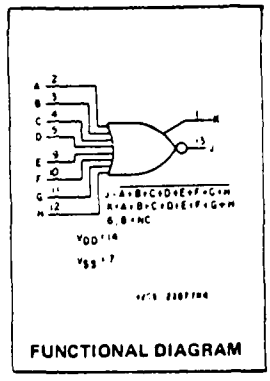
High-Voltage Types (20-Volt Rating)

The RCA-CD4078B NOR/OR Gate provides the system designer with direct implementation of the positive-logic 8-input NOR and OR functions and supplements the existing family of CMOS gates.

The CD4078B types are supplied in 14-lead dual-in-line ceramic packages (D and F suffixes), 14-lead dual-in-line plastic packages (E suffix), 14-lead ceramic flat packages (K suffix), and in chip form (H suffix).

Features:

- Medium-Speed Operation: t_{PHL}, t_{PLH} = 75 ns (typ.) at V_{DD} = 10 V
- Buffered inputs and output
- 5-V, 10-V, and 15-V parametric ratings
- Standardized symmetrical output characteristics
- 100% tested for quiescent current at 20 V
- Maximum input current of 1 μA at 18 V over full package-temperature range: 100 nA at 18 V and 25°C
- Noise margin (over full package-temperature range): 1 V at V_{DD} = 5 V; 2 V at V_{DD} = 10 V; 2.5 V at V_{DD} = 15 V
- Meets all requirements of JEDEC Tentative Standard No. 13A, "Standard Specifications for Description of 'B' Series CMOS Devices"



FUNCTIONAL DIAGRAM

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY-VOLTAGE RANGE, (V_{DD})
(Voltages referenced to V_{SS} Terminal) . . . . . −0.5 to +20 V
INPUT VOLTAGE RANGE, ALL INPUTS . . . . . −0.5 to V_{DD} +0.5 V
DC INPUT CURRENT, ANY ONE INPUT . . . . . ±10 mA
POWER DISSIPATION PER PACKAGE (P_D):
For T_A = −40 to +60°C (PACKAGE TYPE E) . . . . . 500 mW
For T_A = +60 to +85°C (PACKAGE TYPE E) . . . . . Derate Linearly at 12 mW/°C to 200 mW
For T_A = −55 to +100°C (PACKAGE TYPES D, F, K) . . . . . 500 mW
For T_A = +100 to +125°C (PACKAGE TYPES D, F, K) . . . . . Derate Linearly at 12 mW/°C to 200 mW
DEVICE DISSIPATION PER OUTPUT TRANSISTOR
FOR T_A = FULL PACKAGE-TEMPERATURE RANGE (All Package Types) . . . . . 100 mW
OPERATING-TEMPERATURE RANGE (T_A):
PACKAGE TYPES D, F, K, H . . . . . −55 to +125°C
PACKAGE TYPE E . . . . . −40 to +85°C
STORAGE TEMPERATURE RANGE (T_{stg}) . . . . . −65 to +150°C
LEAD TEMPERATURE (DURING SOLDERING):
At distance 1/16 ± 1/32 inch (1.59 ± 0.79 mm) from case for 10 s max. . . . . +265°C

RECOMMENDED OPERATING CONDITIONS

For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	Min.	Max.	Units
Supply Voltage Range (For T_A = Full Package Temperature Range)	3	18	V

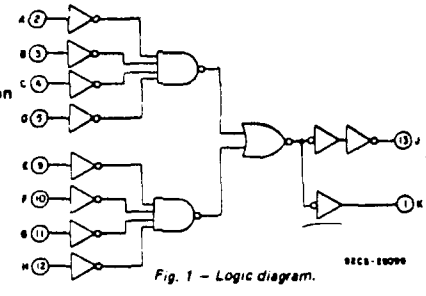


Fig. 1 – Logic diagram.

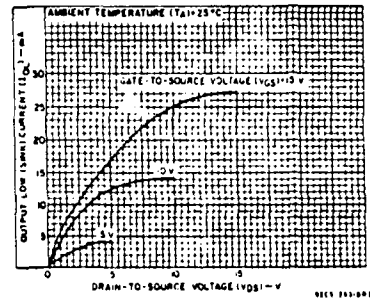


Fig. 2 – Typical output low (sink) current characteristics.

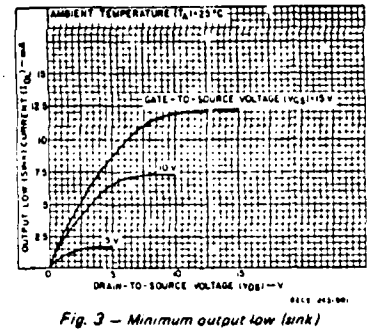


Fig. 3 – Minimum output low (sink) current characteristics.

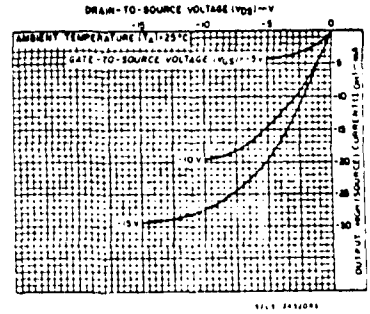


Fig. 4 – Typical output high (source) current characteristics.

DYNAMIC ELECTRICAL CHARACTERISTICS

At T_A = 25°C; Input t_r, t_f = 20 ns, C_L = 50 pF, R_L = 200 kΩ

CHARACTERISTIC	TEST CONDITIONS	ALL TYPES LIMITS			UNITS
		V_{DD} VOLTS	TYP.	MAX	
Propagation Delay Time, t_{PHL}, t_{PLH}		5	150	300	ns
		10	75	150	
		15	55	110	
Transition Time, t_{THL}, t_{TLH}		5	100	200	ns
		10	50	100	
		15	40	80	
Input Capacitance, C_{IN}	Any Input		5	7.5	pF

STATIC ELECTRICAL CHARACTERISTICS

CHARACTERISTIC	CONDITIONS			LIMITS AT INDICATED TEMPERATURES (°C) Values at -55, +25, +125 Apply to D, F, K, H Packages Values at -40, +25, +85 Apply to E Package							UNITS
									+25		
	V_O (V)	V_{IN} (V)	V_{DD} (V)	-55	-40	+85	+125	Min.	Typ.	Max.	
Quiescent Device Current, I_{DD} Max	-	0,5	5	0.25	0.25	7.5	7.5	-	0.01	0.25	μA
	-	0,10	10	0.5	0.5	15	15	-	0.01	0.5	
	-	0,15	15	1	1	30	30	-	0.01	1	
	-	0,20	20	5	5	150	150	-	0.02	5	
Output Low (Sink) Current I_{OL} Min	0.4	0,5	5	0.64	0.61	0.42	0.36	0.51	1		mA
	0.5	0,10	10	1.6	1.5	1.1	0.9	1.3	2.6		
	1.5	0,15	15	4.2	4	2.8	2.4	3.4	6.8		
Output High (Source) Current, I_{OH} Min	4.6	0,5	5	-0.64	-0.61	-0.42	-0.36	-0.51	-1		
	2.5	0,5	5	-2	-1.8	-1.3	-1.15	-1.6	-3.2		
	9.5	0,10	10	-1.6	-1.5	-1.1	-0.9	-1.3	-2.6		
	13.5	0,15	15	-4.2	-4	-2.8	-2.4	-3.4	-6.8		
Output Voltage Low Level, V_{OL} Max	-	0,5	5	0.05					0	0.05	V
	-	0,10	10	0.05					0	0.05	
	-	0,15	15	0.05					0	0.05	
Output Voltage High Level, V_{OH} Min	-	0,5	5	4.95				4.95	5		
	-	0,10	10	9.95				9.95	10		
	-	0,15	15	14.95				14.95	15		
Input Low Voltage, V_{IL} Max	0.5,4.5	-	5	1.5				-	-	1.5	V
	1,9	-	10	3				-	-	3	
	1.5,13.5	-	15	4				-	-	4	
Input High Voltage, V_{IH} Min	0.5,4.5	-	5	3.5				3.5	-	-	
	1,9	-	10	7				7	-	-	
	1.5,13.5	-	15	11				11	-	-	
Input Current I_{IN} Max		0,18	18	±0.1	±0.1	±1	±1	-	$±10^{-5}$	±0.1	μA

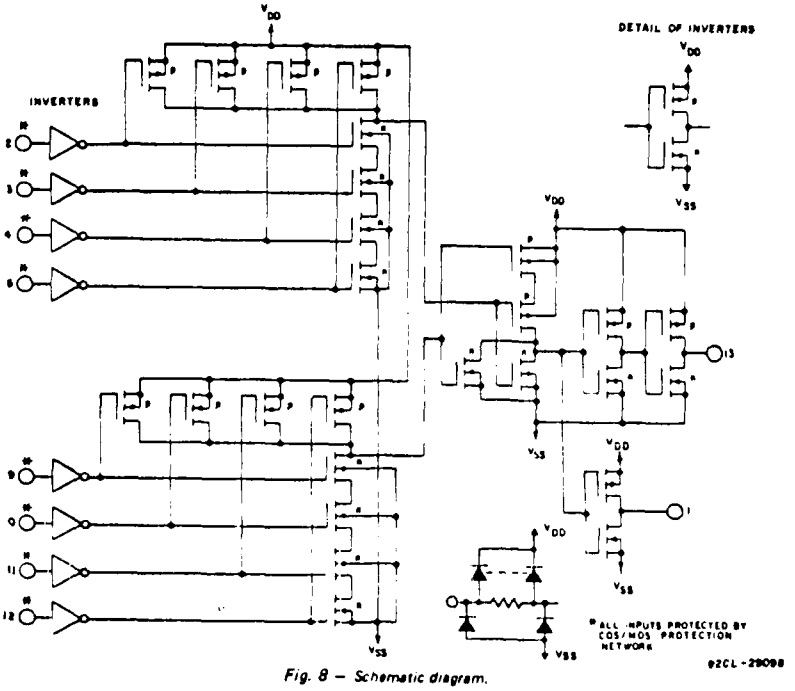


Fig. 8 – Schematic diagram.

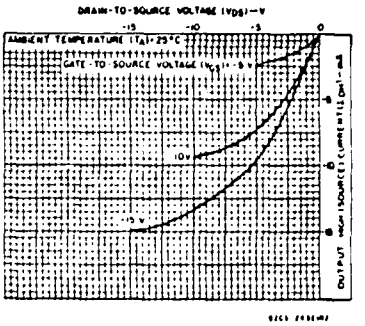


Fig. 5 – Minimum output high (source) current characteristics.

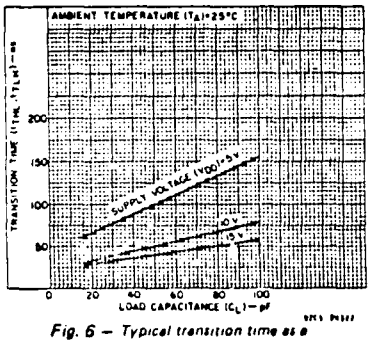


Fig. 6 – Typical transition time as a function of load capacitance.

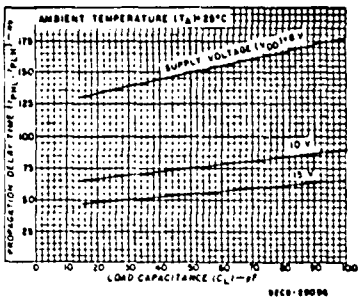


Fig. 7 – Typical propagation delay time as a function of load capacitance.

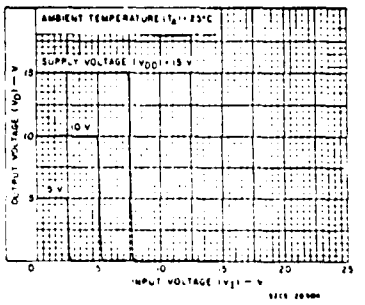


Fig. 9 – Typical voltage transfer characteristics (NOR output).

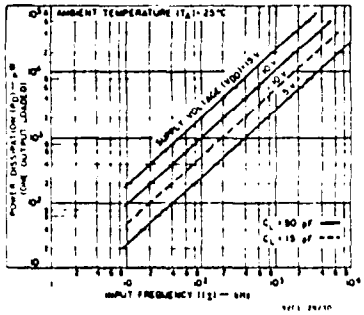


Fig. 10 – Typical dynamic power dissipation as a function of frequency.

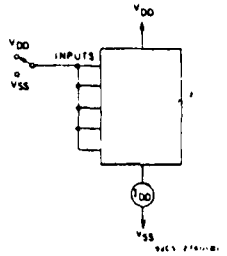


Fig. 11 – Quiescent-device-current test circuit.

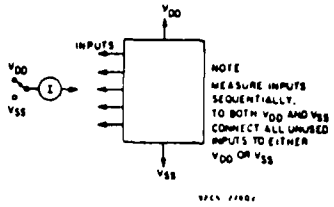


Fig. 12 – Input current test circuit.

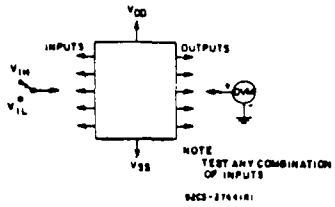


Fig. 13 – Input-voltage test circuit.

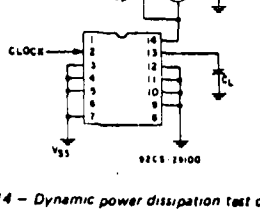
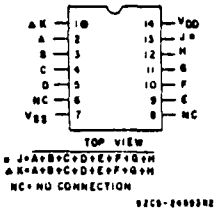
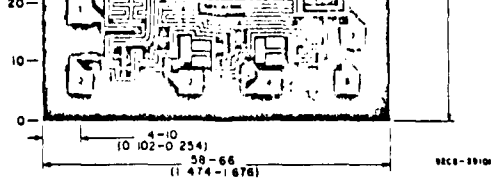


Fig. 14 – Dynamic power dissipation test circuit.



TERMINAL ASSIGNMENT



Dimensions and pad layout for CD4078BH.

Dimensions in parentheses are in millimeters and are derived from the basic inch dimensions as indicated. Grid graduations are in mils (10^{-3} inch).

The photographs and dimensions of each CMOS chip represent a chip when it is part of the wafer. When the wafer is separated into individual chips, the angle of cleavage may vary with respect to the chip face for different chips. The actual dimensions of the isolated chip, therefore, may differ slightly from the nominal dimensions shown. The user should consider a tolerance of −3 mils to +16 mils applicable to the nominal dimensions shown.

E. Multiplexing Circuitry

This appendix gives a design for multiplexing curcuit so the half multiplexed AFIT electrode array can be used. At present a fully working multiplexed 16 x 16 array has not been produced. However, a partially multiplexed version (rows on each column are multiplexed) has been produced and fully tested for functionality. To ultilize the partially multiplexed array with the system developed in this thesis, the column outputs must be multiplexed and a sync pulse must be generated. The system designed to accomplish this is shown in Figure E.1. The design uses a 7 bit binary counter to sequence through a 16 channel multiplexer chip. The circuit reads electrodes across a row by sampling each column, then the array clock is incremented and the next row is read. A sync pulse high is generated when the 0 electrode position is selected and is otherwise low.

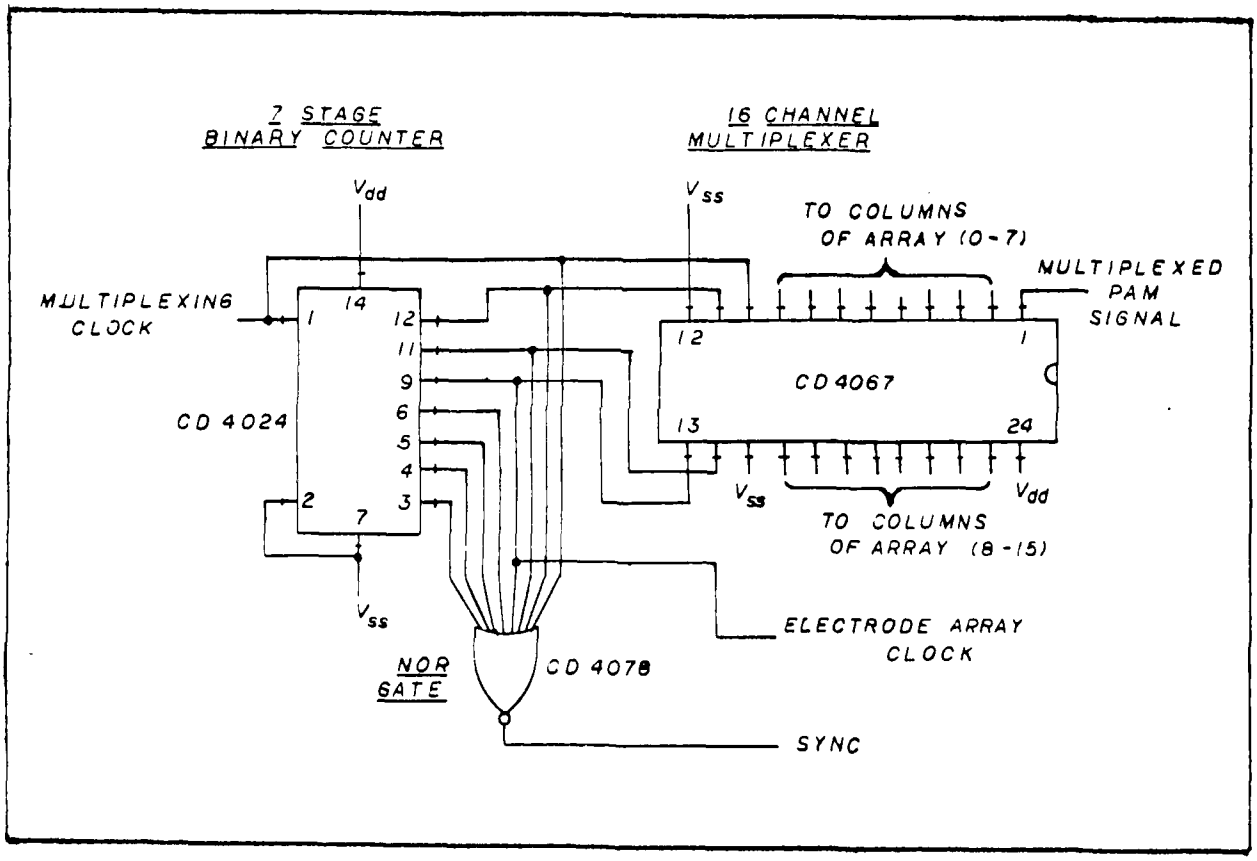


Figure E.1. Multiplexing Circuit

F. Miniaturization Considerations

Overview

To use the design presented in this thesis, the telemetry link must be scalable to allow implantation within a rhesus monkey. To do so requires the use of thick film hybrid circuit layout techniques. Also the problem of biocompatibility must be addressed in both the acceptability of the implant to the host and the ability of the circuit to operate in a harsh environment. Finally, scalable designs must be examined for total system integrity, the ability to operate as designed due to placement, and relative position of individual subsystems in the body. This appendix will describe the necessary considerations for scaling and present useful material to fulfill the design.

Subsystem Placement

To solve the problems noted in the design of internal amplification, FM modulation and support functions, it is necessary to determine proper placement of each subsystem to provide optimum performance of the system. Power supply components, due to their large size and requirement to be close to the skin for inductive coupling, should be placed in the chest cavity. Also the FM modulator circuitry should be placed in the chest cavity in close proximity to the power supply inductive coupling coil to ease implantation and allow the use of the same positioning for coil alignment of both

the powering coil and the FM receiving coil. The array clocking oscillator should be placed as close to the array as possible to prevent the coupling of the oscillator to the inputs of the differential PAM amplifier. Likewise, the amplifier for the PAM signal should be placed close to the array to prevent long leads from generating very large common mode signals and noise in the differential mode signals. Since the sync signal is produced at the electrode array, the sync encoding should also be placed near the electrode array. A proposed system includes a thick film circuit with the amplifier, sync encoder, and the clocking oscillator on a single substrate which can be implanted where the skull is removed to provide access for the electrode array. Another possibility would place the thick film circuit between the skull and the skin allowing a slight bulge in the head there. The signals from the array; multiplexed output, sync, and reference electrode can be wired to the hybrid circuit with very short runs while less sensitive signals like the modulating signal and power supply lines will run down the neck and into the chest cavity where it will join the power supply and modulator. Size requirements in the chest cavity are less critical so power supply and modulator circuits can be placed on small scale printed circuit boards and enclosed with the batteries for implantation. If needed, the multiplexer circuit of Appendix E can be placed on the same thick film as the amplifier, sync encoder, and clocking oscillator. If the design becomes to bulky for implantation

in the head the amplifier, clocking oscillator, sync encoder and possibly row multiplexer thick film circuit can be moved to the power supply. This is not advantageous because long wire runs to the electrode array promote noise and coupling between signals

Thick Film Circuit

The realization of a thick film circuit for implantable circuits requires small size, good circuit stability in a hostile environment and hermetic sealing to prevent moisture and ion degradation (41:26). Integrated circuit used in the design should be either the bare chip or a leadless chip carriers. The leadless chip carrier is preferred because the package provides a hermetical seal, but at the expense of area used on the thick film substrate. All circuits used in the design are available in either bare chip or leadless chip carrier as stated by the data sheets, however lead times may be severe. The substrate used to make the thick film circuit is usually alumina which provides good structural rigidity. Conductor and resistor patterns are printed directly onto the substrate as pastes applied by screen printing methods. Conductors are pastes made of precious metals in an organic binder while resistor pastes are mixtures of conductor and glass in a similar binder (42:194). Resistances range easily from 1 ohm to 10 megohms using thick film, however, tolerances of only + or - 10% can be achieved. Since the design requires precision resistances and fairly high

resistances, it is recommended that cermet chip resistors be used in series with small trimable thick film resistors. High precision resistors used in the PAM amplifier are commonly available in 1% tolerances. Trimming of resistors can add to the common mode rejection so the design should incorporate trimable resistors in the first and second stages of the PAM amplifier. Variable resistors also can be achieved by trimming once suitable starting resistances are known. Thick film capacitors are only good for small values, so discrete ceramic chip capacitors should be used in the design. Simple reflow soldering provides adequate electrical connections to the thick film conducting patterns for discrete components and leadless chip carriers while wire bonding gives good results for unpackaged integrated circuits. Connections out of the thick film packaging to the array and power supply are made by drilling holes through the alumina substrate and passing stainless steel wires through the holes. Glass pastes fill in the voids left in the holes and provide a hermetic seal to the outside when fired (41:32).

To prevent moisture and ion damage to the thick film circuit, passivation methods must be used on the circuit before the package is hermetically sealed. Glass dielectric overglazes on the thick film circuits with opening for connections provides suitable protection for thick film conductors and trimmed resistors (43:40). IC's should then be put in place and interconnection made to thick conductors.

Two component epoxy resins, mixed under partial vacuum in a low humidity nitrogen saturated atmosphere are applied to IC's and allowed to cure (41:31-32). An ion barrier layer of polyimide is then placed over the previously cured epoxy, and it is cured. Special care must be taken to insure openings for discrete component connections are kept open. Discrete components are then reflow soldered to the conductor patterns and an epoxy over coat applied to the entire component side of the circuit. Passivation and ion barriers are complete and the circuit is ready for hermetic sealing.

Hermetical sealing of the package is necessary to inhibit the penetration of fluid into the device. Techniques include total encapsulation in glass, box like containers using stainless steel or titanium, dipping in polymers, and covers using the alumina substrate for the backing. For ease of use, the latter will be described. A cover is manufactured out of gold to fit snugly over the components so the sides extend down beyond the bottom of the substrate. A hole is placed in the cover to allow back filling of inert helium gas in to the sealed unit and will be soldered (Pb-Sn-Ag) shut once the helium is present. The bottom is sealed by soldering a fillet in between the gold cover and a Pt-Au metalization which was placed on the bottom of the substrate before thick film processing (44:401). This provides a suitable hermetic seal and a good foundation to make the units biocompatible.

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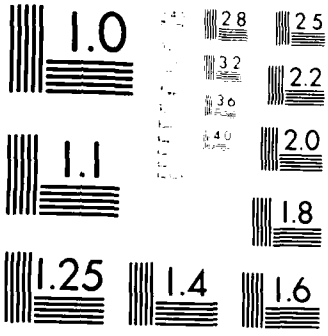

Biocompatibility

Biocompatibility allows the implant to be accepted by surrounding tissue and provides no contaminates or tissue damage from materials or shapes. Previous efforts have used a full assortment of biocompatible encapsulents including waxes, plastics, epoxies, and polymers but none have proved as useful as the silicon rubber. Silicon rubber provides some very good characteristics for an insulative encapsulent. First silicon rubber has been used subdermally for many years with only minimal reaction from the surrounding tissue (45:34). This provides a good biological foundation for the implanted device by allowing no defense mechanisms to disrupt the normal function. Secondly, the silicon rubber does allow limited water vapor penetration. The amount of penetration is low enough that insulating capabilities are preserved and failure does not occur due to interlead current paths. Here the importance is to make sure the encapsulent forms a tight adhesion to the leads and package. Voids formed by poor adhesion form shunt current paths which result in implantation failure (46:219). Silicon rubber has good adhesion characteristics, and with wetting agents and clean binding surfaces a good seal is assured. Void generation within the silicon rubber can cause problems, so rubber curing should be done in a light vacuum so aeration can occur. Objects that are sealed this way should have smooth edges and avoid concave surfaces. This is because skrinkage occurs upon curing.

Once properly encapsulated the site of implantation must be carefully selected to keep the implant stationary and not cause damage while allowing proper operation. Receiving and transmission coils must be at the surface while battery pack and transmission circuitry are placed with the chest cavity affixed to a bone to prevent movement. Brain circuitry placement requires light pressure of the array on the brain surface while the amplifier and oscillator placement is outside of the skull or takes the place of the skull making sure not to exert any pressure on the brain. Teflon coated stainless steel wire used for interconnections should run just under skin from the brain to the transmitter unit and penetrate the chest cavity just at the point of where the implant is. At all times routing and placement must conform with the need for unrestrained natural functioning of the host. The circuit can be implanted and used over a period of several years before requiring surgery for replacement and overhaul. At the time of replacement, the previously implanted device should be analyzed to determine cause of failure and the knowledge used to generate better implantable devices.

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The research conducted in this study develops an implantable communications (biotelemetry) link for the Air Force Institute of Technology's implantable, multiplexed, multielectrode array used to record electric potentials on the visual cortex of a mammal. A prototype is developed to test the feasibility of transcutaneous data transfer and power transfer for a system relaying 100 KHz of data bandwidth. The working system uses a varactor FM modulator, phase locked loop demodulator, and op amp signal amplification. Power transfer is made by a single frequency RF inductive couple to an implanted rechargable Ni-Cd battery pack. The implanted system draws 18 milliwatts of power and the power supply is capable of supplying 30 milliamps of current at 5volts for a 2 hour period before recharging is required. Details of the design procedures as well as recommendations for an implantable system realization are included.

Item 18.

Electrode Array
Operational Amplifiers
Voltage Controlled Oscillators
Bioengineering
EEG
Varactor Diodes
Recording System
Biotelemetry
Power Supplies

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